


Hardware-Software Contracts for Safe and Secure Systems

Jan Reineke @  UNIVERSITÄT
DES
SAARLANDES

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The Need for New HW/SW Contracts

“Stone-age” Computing

Applications implemented data transformations:
e.g. payroll processing

Hardware:

- isolated, on-site
- limited interaction with environment

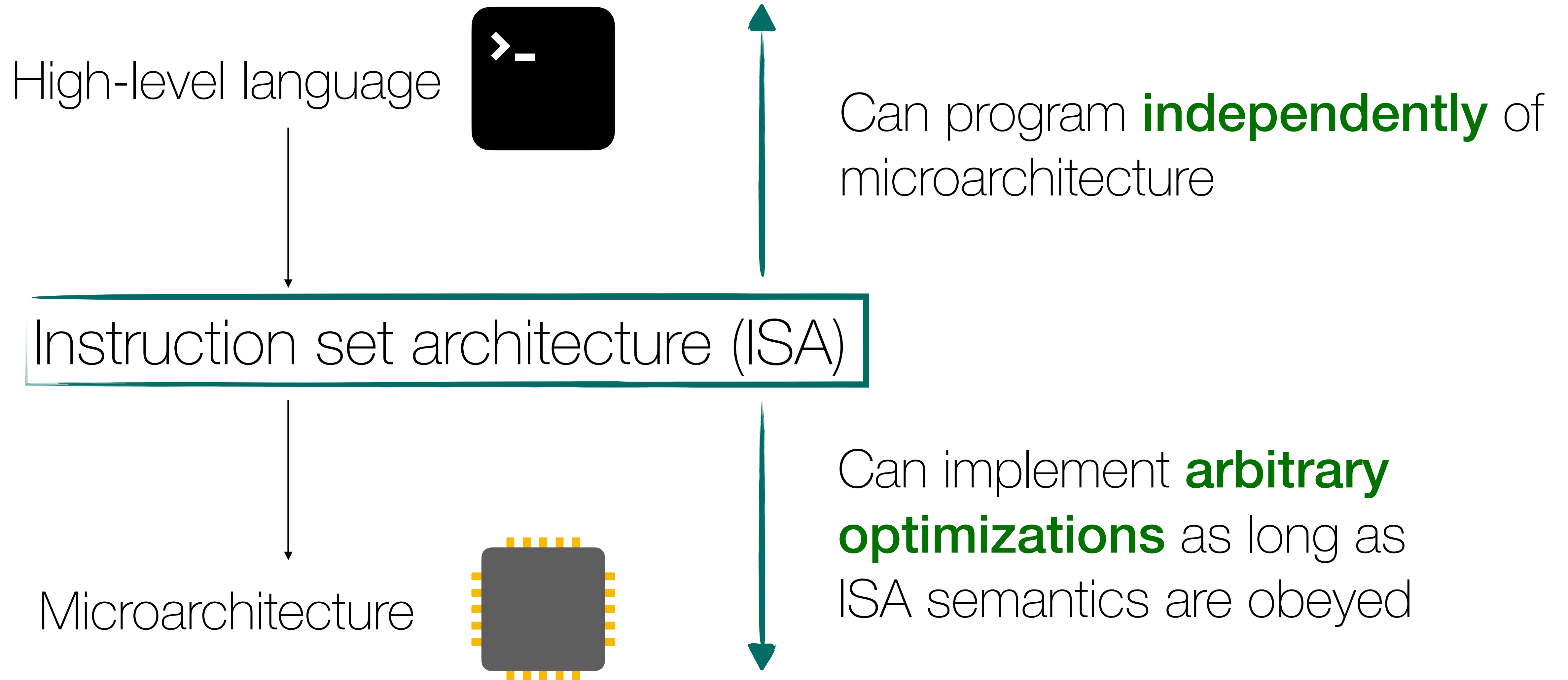
IBM System 360/30



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HW/SW Contract: Instruction set architecture (ISA)

ISA: Benefits



“Modern” (?) Computing

Applications are:

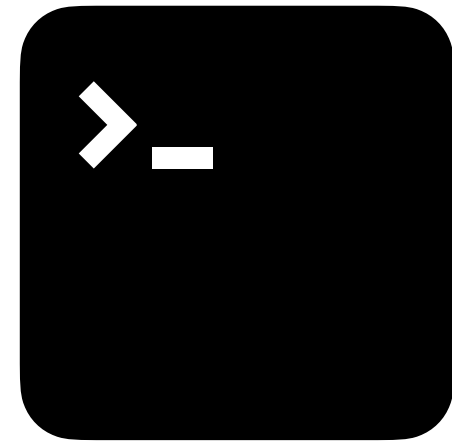
- **Data-driven**: e.g. deep neural networks
- **Distributed**: e.g. locally + in the cloud
- **Open**: e.g. untrusted code in the browser 
- **Real-time**: interacting with the physical environment 

What are the implications for HW/SW contracts?

Inadequacy of the ISA: Real-time Systems



High-level language

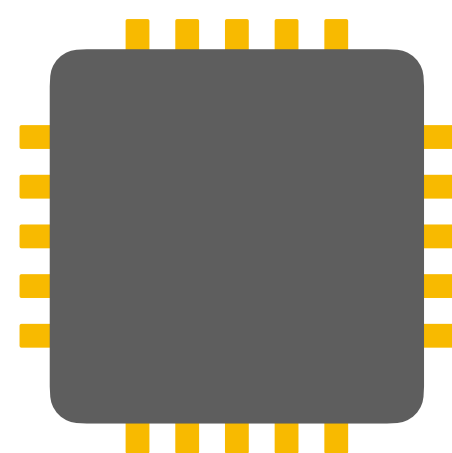


Impossible to program
real-time systems on top of ISA

Instruction set architecture (ISA)

Abstracts from time
No control over time

Microarchitecture



Can implement arbitrary
unpredictable optimizations as long
as ISA is implemented correctly

***Wanted:* Timed HW/SW Contracts**



Programs have a **timed semantics** that is **efficiently predictable**
Programs have **control** over timing

Timed Instruction Set Architecture

Admit a **wide range** of **timing-predictable**, yet high-performance
microarchitectural **implementations**

Wanted: Timed HW/SW Contracts



Some answers:

E. Lee, J. Reineke, and M. Zimmer:

Abstract PRET Machines

RTSS 2017

Determinism

S. Hahn and J. Reineke:

Design and Analysis of SIC:

A Provably Timing-Predictable Pipelined Processor Core

RTSS 2018 (🏆 Best Student Paper Award)

Monotonicity

G. Stock, S. Hahn and J. Reineke:

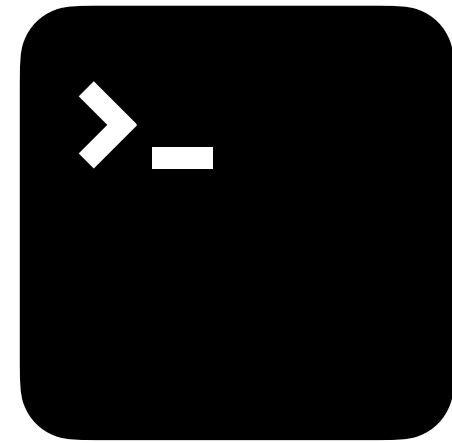
Cache Persistence Analysis: Finally Exact

RTSS 2019 (🏆 Best Paper Award)

Inadequacy of the ISA: Side channels



High-level language

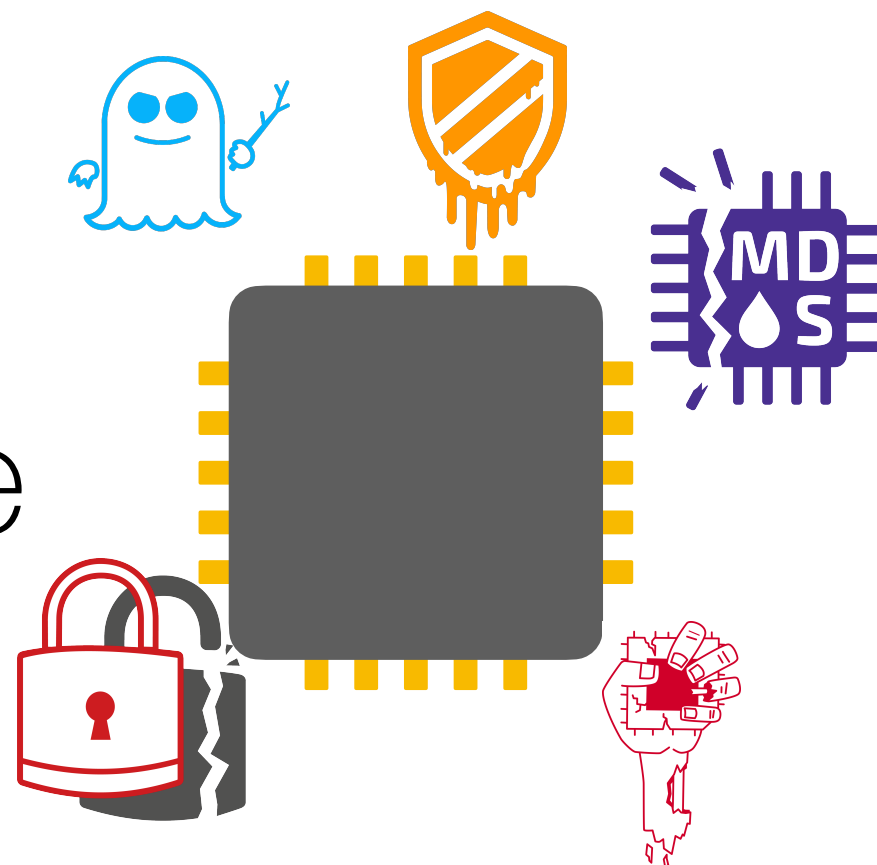


Impossible to program securely
cryptographic algorithms?
sandboxing untrusted code?

Instruction set architecture (ISA)

**No guarantees
about side channels**

Microarchitecture



Can implement arbitrary **insecure**
optimizations as long as
ISA is implemented correctly

A Way Forward: HW/SW Security Contracts



Can program **securely** on top of contract
independently of microarchitecture

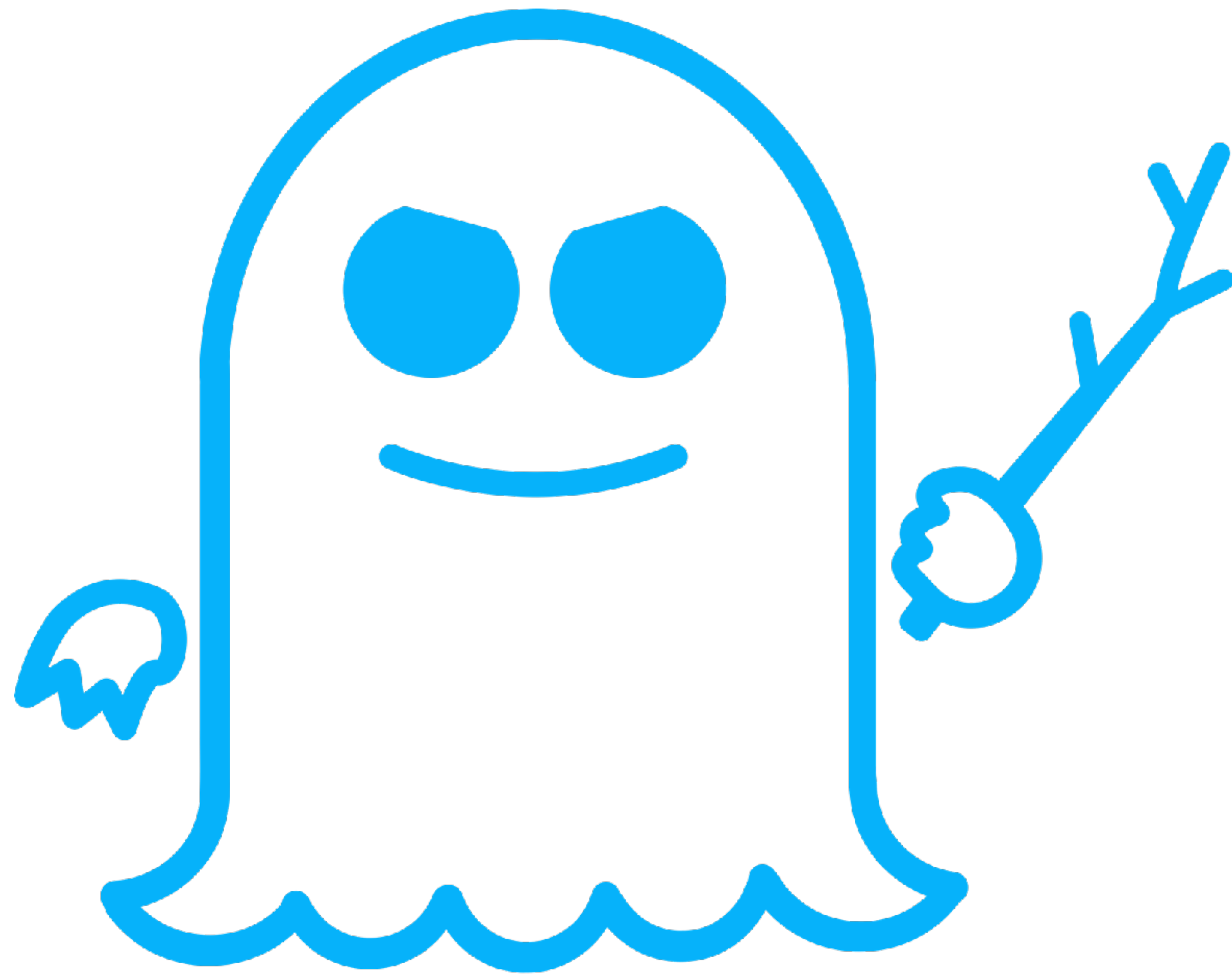
HW/SW contract = ISA + X

**Succinctly captures
possible information leakage**



Can implement **arbitrary insecure optimizations**
as long as contract is obeyed

A Concrete Challenge: Spectre



SPECTRE

Exploits *speculative execution*

Almost *all* modern *CPUs*
are *affected*

Example: Spectre v1 Gadget

x is out of bounds

Executed speculatively

```
1. if (x < A_size)  
2.   y = A[x]  
3.   z = B[y*512]  
4. end
```

Access “secret” **A**[**x**]

Transmit **A**[**x**] via data cache

Hardware Countermeasures

InvisiSpec: Making Speculative Execution
Invisible in the Cache

Mengjia Yan[†], Jiho Choi[†], Dimitrios Skarlatos, Adnan
University of Illinois at Urbana-Champaign
{myan8, jchoi42, skarlat2}@illinois.edu

Ofir Weisse
University of Michigan

Thomas F. Wenisch
University of Michigan

Ian Neal
University of Michigan

Baris Kasikci
University of Michigan

Kevin Loughlin
University of Michigan

CleanupSpec: An “Undo” Approach to Safe Speculation

Gururaj Saileshwar
gururaj.s@gatech.edu
Georgia Institute of Technology

Moinuddin K. Qureshi
moin@gatech.edu
Georgia Institute of Technology

Speculative Taint Tracking (STT): A Comprehensive Protection
for Speculatively Accessed Data

Mengjia Yan
University of Illinois at
Urbana-Champaign
myan8@illinois.edu

Josep Torrellas
University of Illinois at
Urbana-Champaign

Artem Khyzha
Tel Aviv University
artkhyzha@mail.tau.ac.il

Christopher W. Fletcher
University of Illinois at
Urbana-Champaign

Efficient Invisible Speculative Execution through
Selective Delay and Value Prediction

Georgios Sakalis
University of Michigan

Stefanos Kaxiras
Uppsala University
Uppsala, Sweden
stefanos.kaxiras@it.uu.se

Magnus Sjalander
Norwegian University of Science and
Technology
Trondheim, Norway
magnus.sjalander@ntnu.no

Alberto Ros
University of Murcia
Murcia, Spain
aros@ditec.um.es

Examples

```
1.  if (x < A_size)
2.      y = A[x]
3.      z = B[y*512]
4.  end
```

Delay loads until
they can be retired
[Sakalis et al., ISCA'19]

Delay loads until they cannot
be squashed
[Sakalis et al., ISCA'19]

Taint speculatively loaded data
+ delay tainted loads
[STT and NDA, MICRO'19]

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What security
properties do HW
countermeasures
enforce?

How can we program
securely?

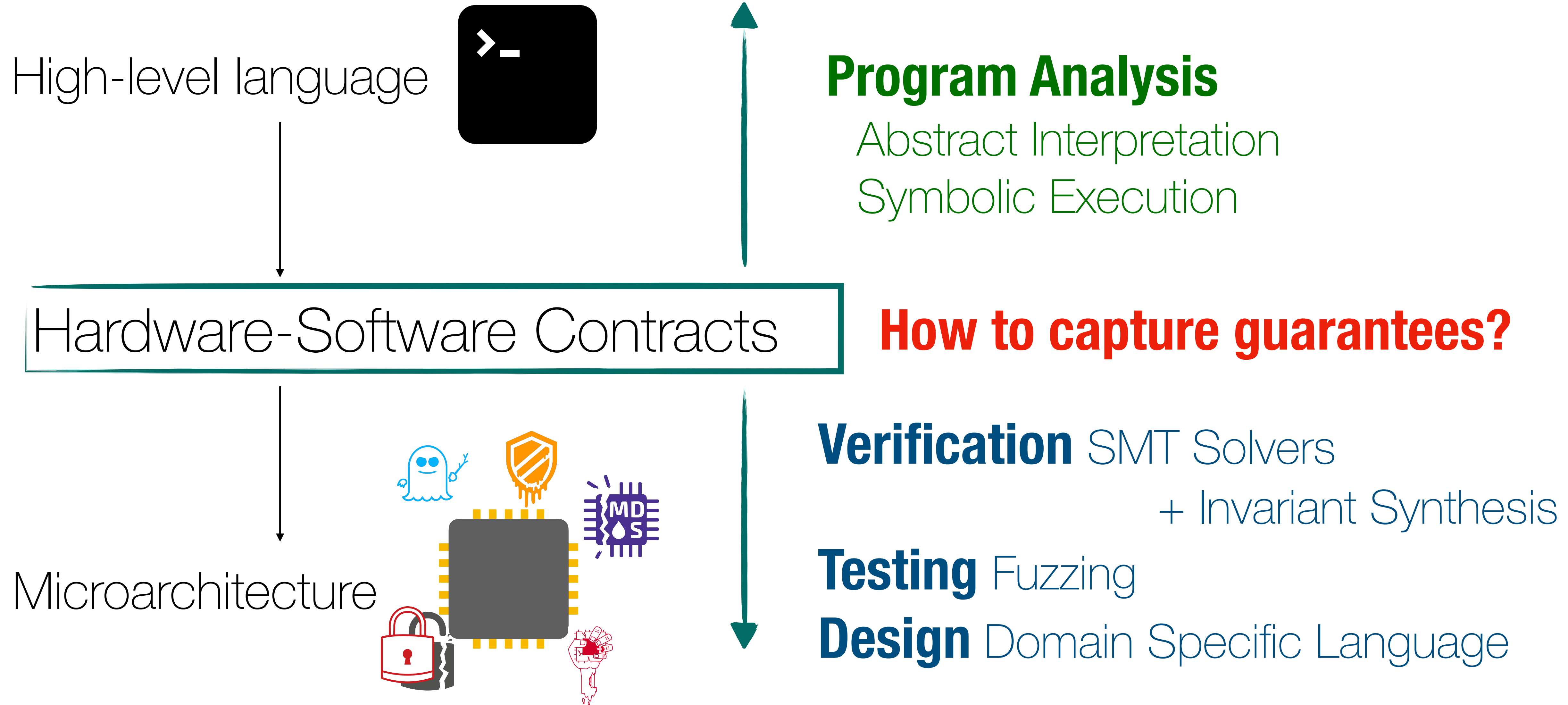
Some Answers:

M. Guarnieri, B. Köpf, J. Reineke, and P. Vila

Hardware-Software Contracts for Secure Speculation

S&P (Oakland) 2021 ( Best Paper Award)

Research Landscape around HW/SW Contracts



Happy to chat about PhD and internship opportunities

Thank you for your attention