How to get decidability of distributed synthesis ?

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Joint work with Thomas Chatain and Nathalie Sznajder

March 12, 2009
Séminaire Bordeaux

Outline

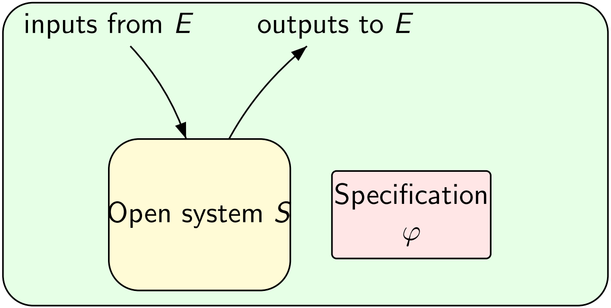
1 Introduction

2 Model

3 Specification

4 Decidability Results

Synthesis of a reactive system



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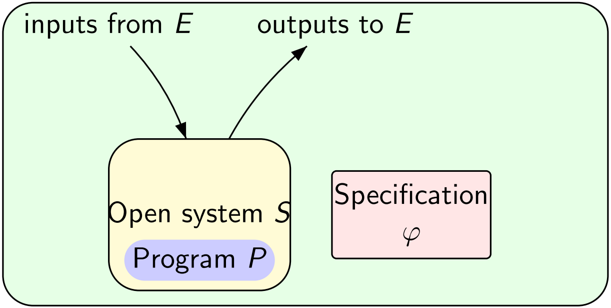
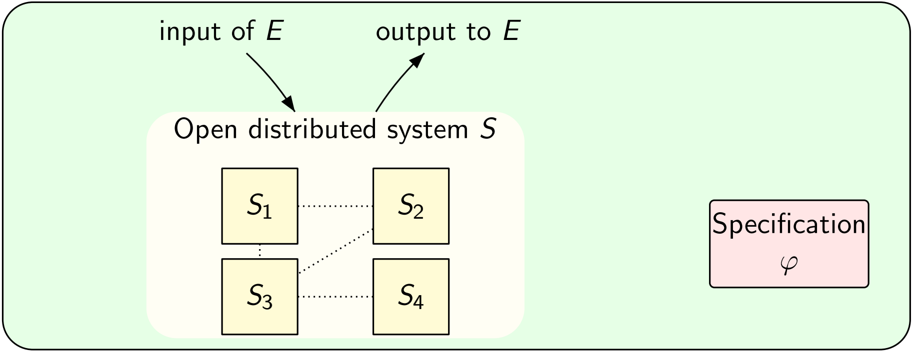


Two problems

- Decide whether there exists a program st. $P \| E \models \varphi, \quad \forall E$.
- Synthesis: If so, compute such a program.

For reasonable systems and specifications, the problems are decidable.

Distributed synthesis



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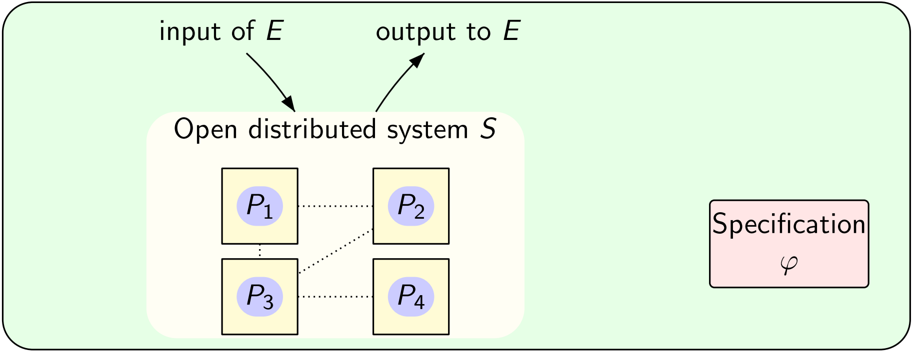

Two problems

- Decide the existence of a distributed program such that their joint behavior $P_1||P_2||P_3||P_4||E$ satisfies φ, for all E.
- Synthesis : If it exists, compute such a distributed program.

Distributed synthesis: Undecidable in general!?

Synchronous semantics: Introduced by Pnueli Rosner '90

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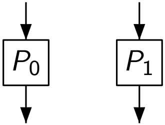

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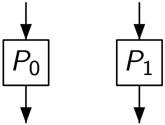
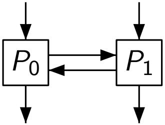
- Undecidable with global specifications.
- Undecidable with constraints on internal channels.





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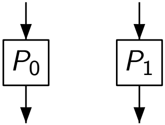

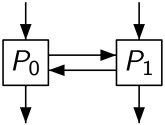

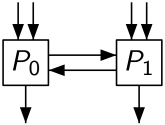

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- At each tick of a global clock, all processes and the environment output their new value
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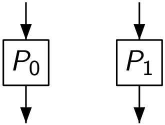
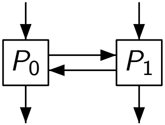
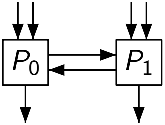
- Undecidable with bandwidth constraints.
- Decidable for some architectures, e.g., pipelines.







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P.G., Benjamin Lerman, Marc Zeitoun

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Theorem

Synthesis problem is decidable for co-graph dependence alphabets, i.e., for series-parallel systems.

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Our model

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  - will not restrain communication abilities

Decidability Results

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Synthesis problem is decidable for

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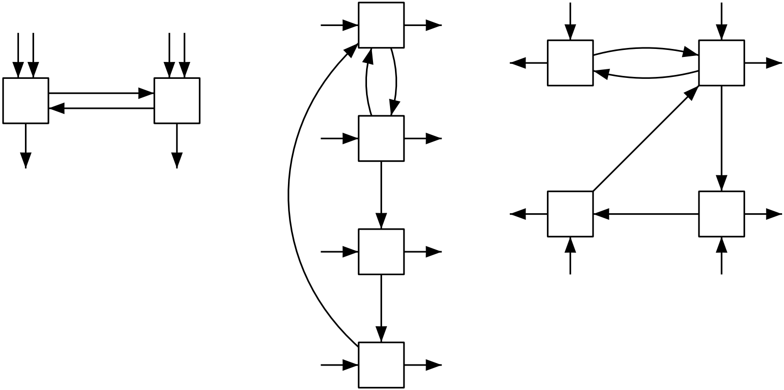

Decidability Results

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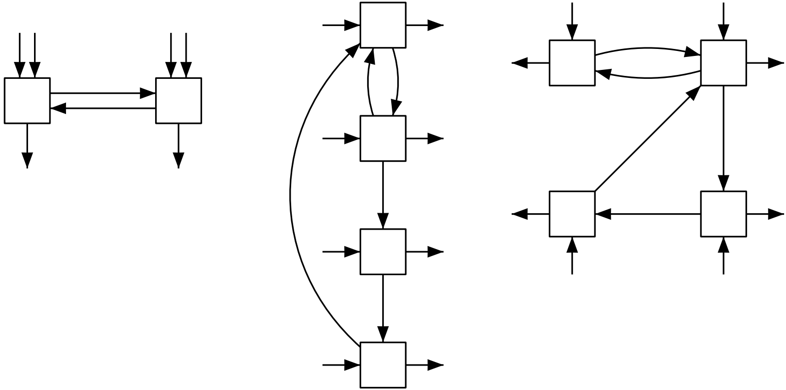
Synthesis problem is decidable for

- strongly-connected architectures,
- disjoint unions of decidable architectures.



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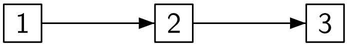

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- Communication graph $(Proc, E)$
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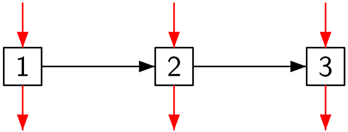

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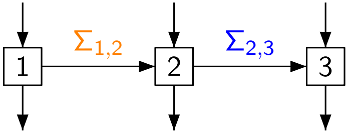

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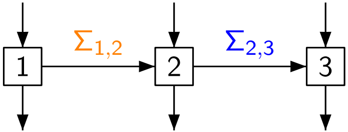

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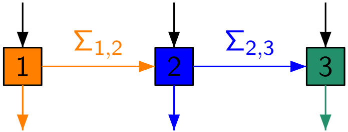
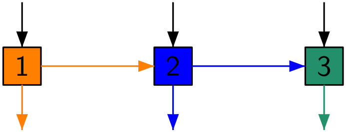
- For each process i,
  $\Sigma_i^c = \mathrm{Out}_i \cup \bigcup_{j,(i,j) \in E} \Sigma_{i,j}$ is the set of signals it can send (control),
  $\Sigma_i = \mathrm{In}_i \cup \Sigma_i^c$ is its alphabet.

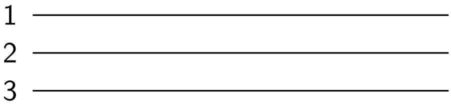


The model: runs

Runs

A run is a Mazurkiewicz trace $t = (V, \lambda, \leq)$ over (Σ, D)
where $a \; D \; b$ if there is a process that takes part both in a and b





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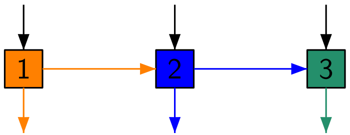

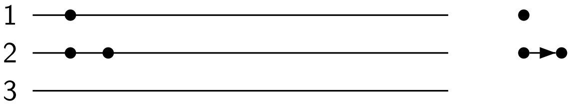

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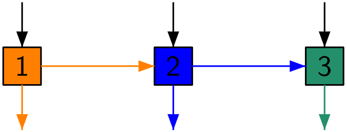

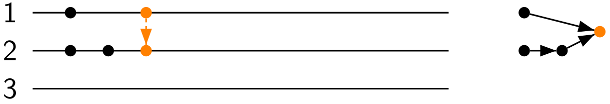

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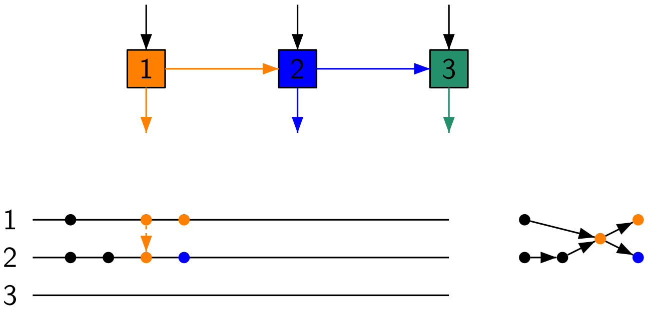

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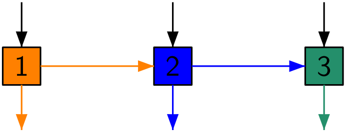

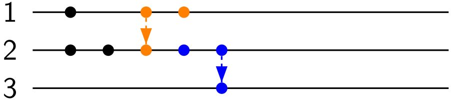

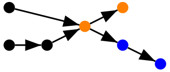

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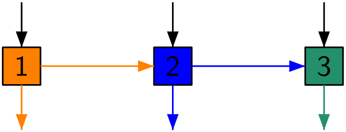

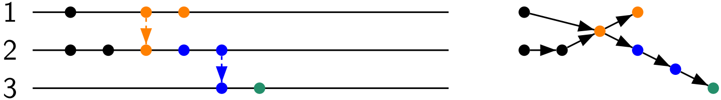

The model: strategies

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- Strategies are partial functions $f_i : \Sigma_i^* \to \Sigma_i^c$ with local memory.

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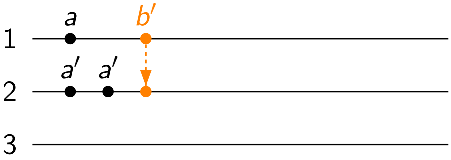

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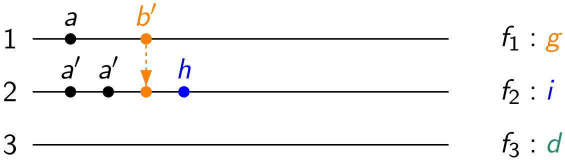

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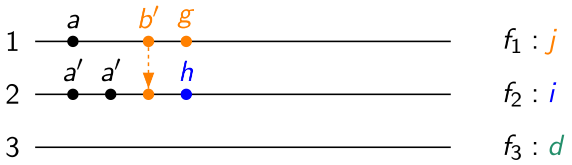

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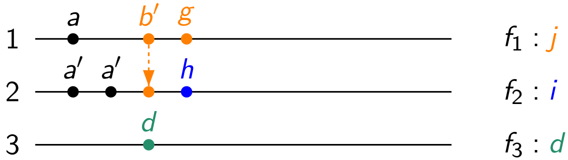

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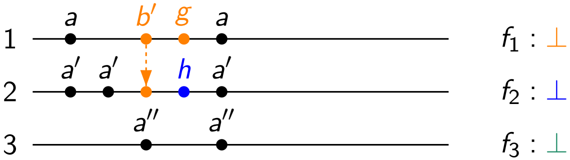
- A run $t = (V, \lambda, \leq)$ is f-maximal if for each process i either $V_i = \lambda^{-1}(\Sigma_i)$ is infinite, or f_i is undefined on the maximal event of V_i.



The model

Observable runs

Given a run $t = (V, \lambda, \leq)$, we define the observable run by

$$\pi_\Gamma(t) = (\Gamma, \lambda_{|\Gamma}, \leq \cap (\Gamma \times \Gamma))$$

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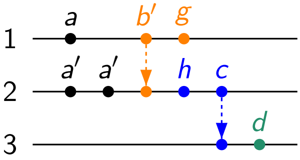

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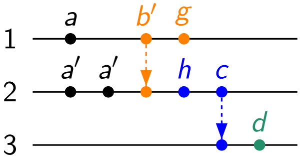

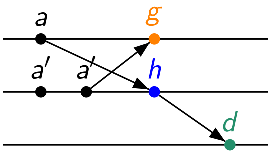

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If so, compute them

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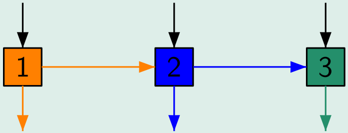

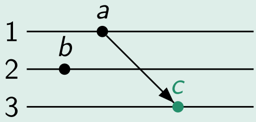

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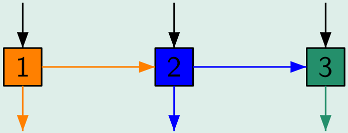

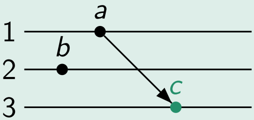

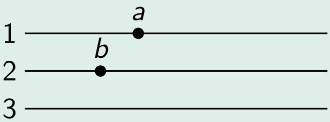

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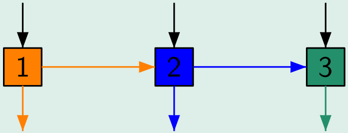

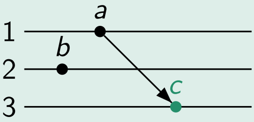

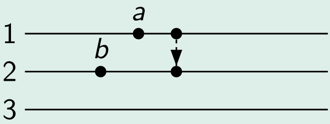

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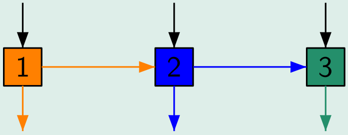

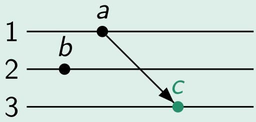

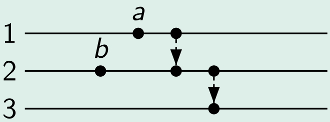

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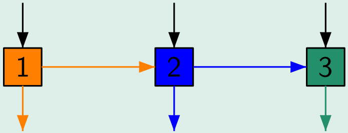

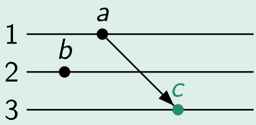

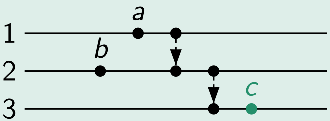

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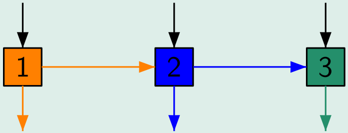

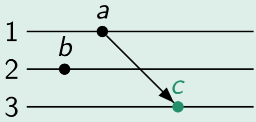

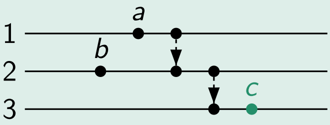

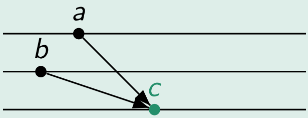

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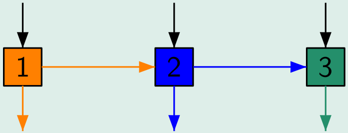

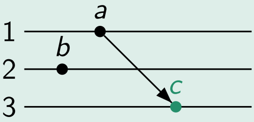

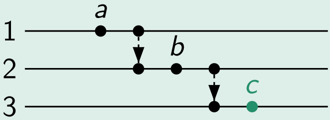

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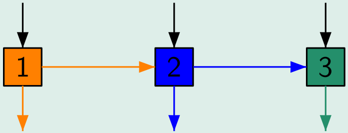

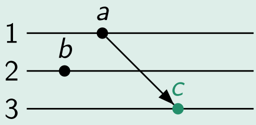

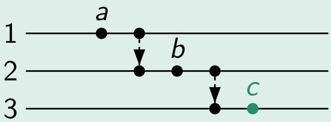

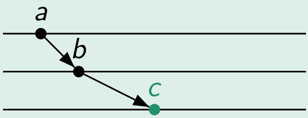

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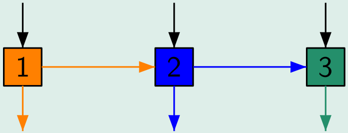

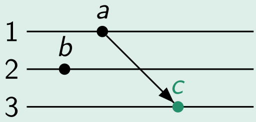

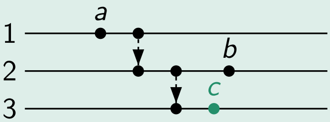

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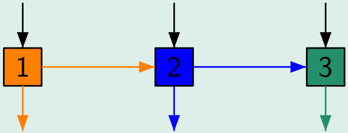

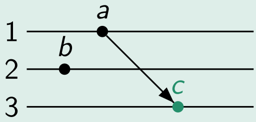

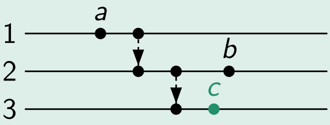

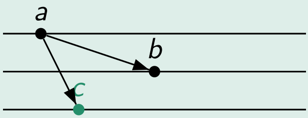

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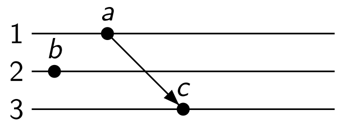

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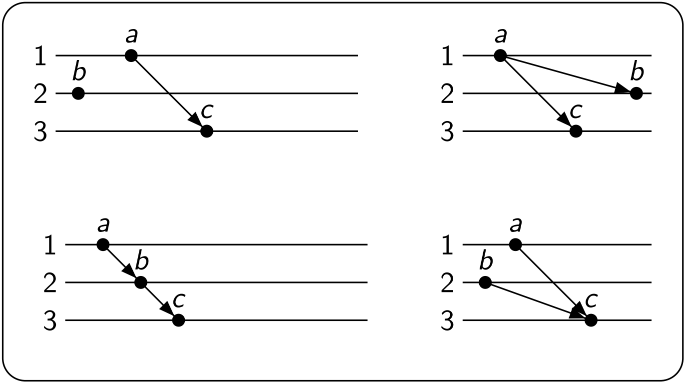

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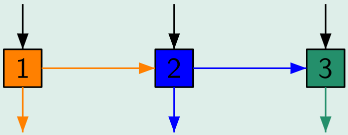

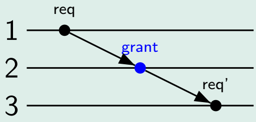

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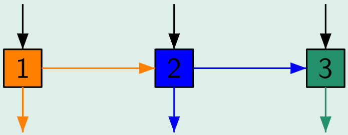

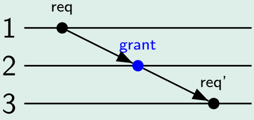

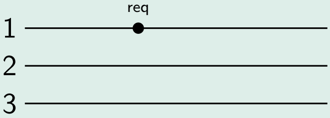

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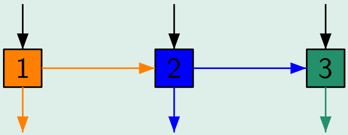

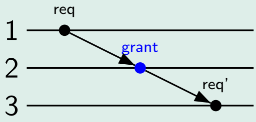

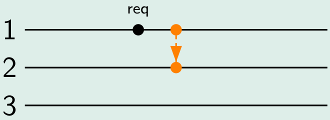

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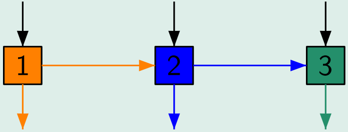

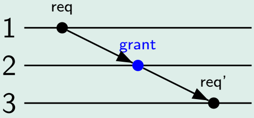

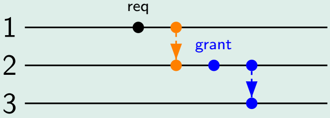

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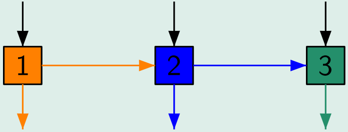

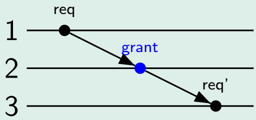

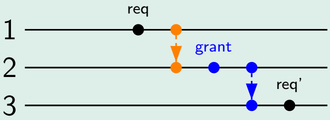

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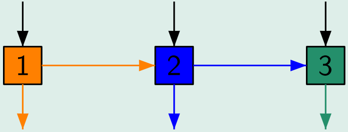

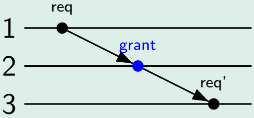

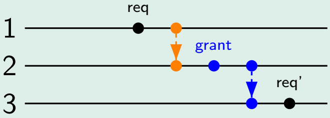

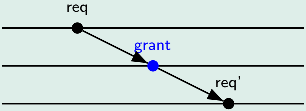

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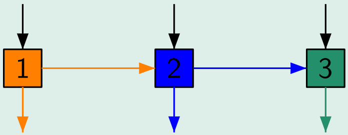

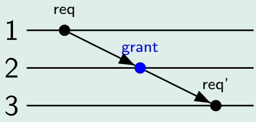

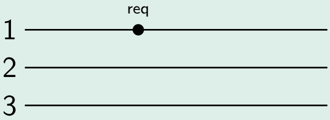

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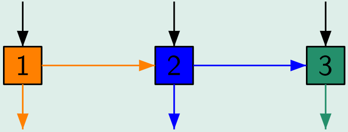

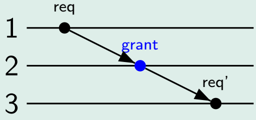

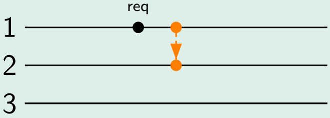

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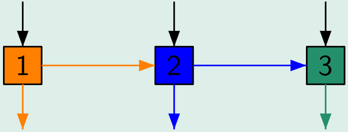

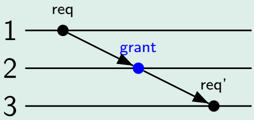

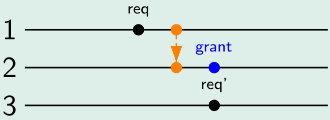

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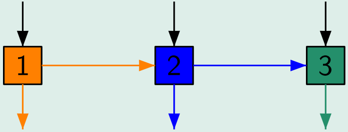

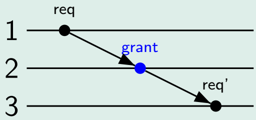

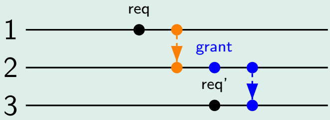

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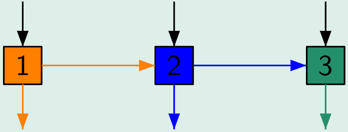

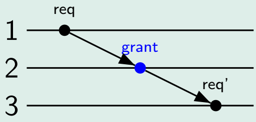

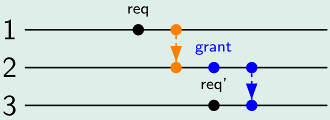

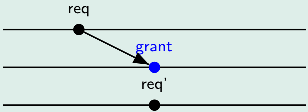

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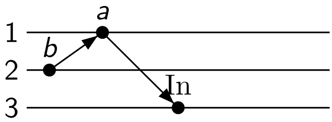

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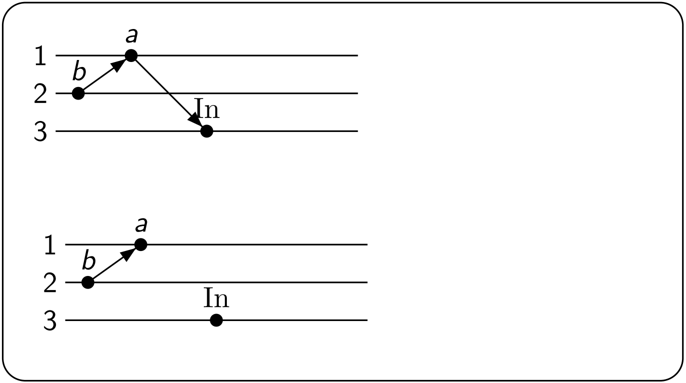


Example of a logic closed by extension and weakening

AlocTL

$$
\begin{aligned}
\varphi ::= a \mid \neg a \mid \varphi \vee \varphi \mid \varphi \wedge \varphi \\
&\mid \mathsf{X}_i\, \varphi \mid \varphi\, \mathsf{U}_i\, \varphi \mid \neg\, \mathsf{X}_i \top \mid \varphi\, \widetilde{\mathsf{U}}_i\, \varphi \\
&\mid \mathsf{Y}_i\, \varphi \mid \varphi\, \mathsf{S}_i\, \varphi \mid \neg\, \mathsf{Y}_i \top \mid \varphi\, \widetilde{\mathsf{S}}_i\, \varphi \\
&\mid \mathsf{F}_{i,j}(\mathrm{Out} \wedge \varphi) \mid \mathrm{Out} \wedge \mathsf{H}_{i,j}\, \varphi
\end{aligned}
$$

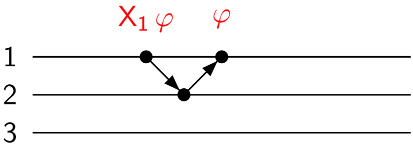
with $a \in \Gamma$ and $i, j \in \mathrm{Proc}$

Example of a logic closed by extension and weakening

AlocTL

$$\begin{aligned}\varphi ::= a \mid \neg a \mid \varphi \vee \varphi \mid \varphi \wedge \varphi \\ \mid \mathsf{X}_i\, \varphi \mid \varphi\, \mathsf{U}_i\, \varphi \mid \neg\, \mathsf{X}_i \top \mid \varphi\, \widetilde{\mathsf{U}}_i\, \varphi \\ \mid \mathsf{Y}_i\, \varphi \mid \varphi\, \mathsf{S}_i\, \varphi \mid \neg\, \mathsf{Y}_i \top \mid \varphi\, \widetilde{\mathsf{S}}_i\, \varphi \\ \mid \mathsf{F}_{i,j}(\mathrm{Out} \wedge \varphi) \mid \mathrm{Out} \wedge \mathsf{H}_{i,j}\, \varphi\end{aligned}$$

with $a \in \Gamma$ and $i, j \in \mathrm{Proc}$



Example of a logic closed by extension and weakening

AlocTL

$$\begin{aligned}\varphi ::= {} & a \mid \neg a \mid \varphi \vee \varphi \mid \varphi \wedge \varphi \\ & \mid \mathsf{X}_i\, \varphi \mid \varphi\, \mathsf{U}_i\, \varphi \mid \neg\, \mathsf{X}_i \top \mid \varphi\, \widetilde{\mathsf{U}}_i\, \varphi \\ & \mid \mathsf{Y}_i\, \varphi \mid \varphi\, \mathsf{S}_i\, \varphi \mid \neg\, \mathsf{Y}_i \top \mid \varphi\, \widetilde{\mathsf{S}}_i\, \varphi \\ & \mid \mathsf{F}_{i,j}(\mathrm{Out} \wedge \varphi) \mid \mathrm{Out} \wedge \mathsf{H}_{i,j}\, \varphi\end{aligned}$$

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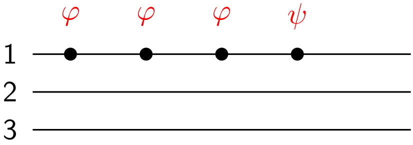

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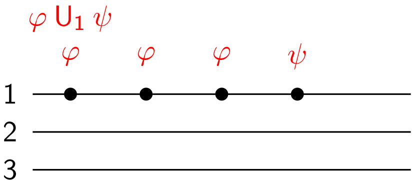

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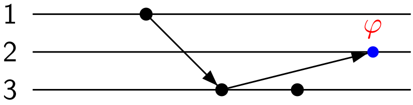

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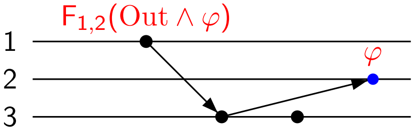

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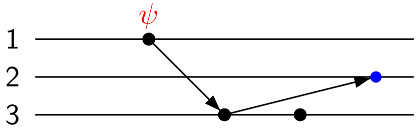

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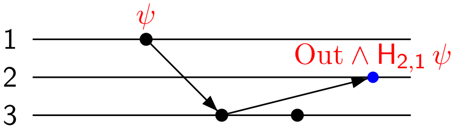

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Formulae

- $\mathsf{G}_1(\mathtt{request} \longrightarrow \mathsf{F}_{1,2}(\mathrm{Out} \wedge \mathtt{grant}))$
- $\mathsf{G}_2(\mathtt{grant} \longrightarrow (\mathrm{Out} \wedge \mathsf{H}_{2,1}\, \mathtt{request}))$

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Theorem

AlocTL is closed under extension and weakening

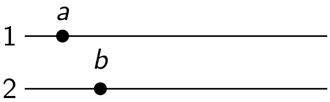
Closure by extension

- $\neg\, \mathsf{F}_{i,j}\, \varphi$ forbidden!

Closure by extension

- $\neg\, \mathrm{F}_{i,j}\, \varphi$ forbidden!

$a \wedge \neg\, \mathrm{F}_{1,2}\, b$



OK

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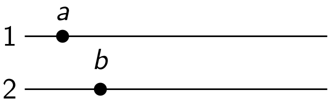
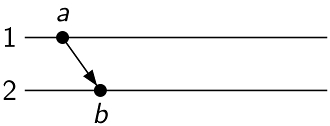


OK



KO

Closure by extension

- $\neg \mathsf{F}_{i,j}\,\varphi$ forbidden!
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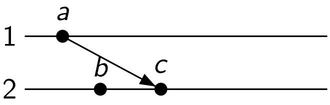

$a \wedge \mathrm{X}_{1,2}\, c$

OK

Closure by extension

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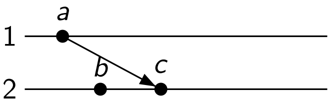
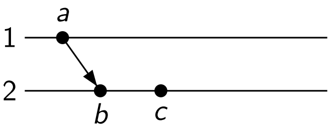


OK



KO

Closure by extension

- $\neg \mathsf{F}_{i,j}\, \varphi$ forbidden!
- $X_{i,j}\varphi$ forbidden!

Specification is not allowed to require concurrency

Closure by extension

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Specification is not allowed to require concurrency

Closure by weakening

Ensured by $\mathsf{F}_{i,j} \wedge \mathrm{Out}$ and $\mathrm{Out} \wedge \mathsf{H}_{i,j}\,\varphi$.

Outline

1. Introduction
2. Model
3. Specification
4. Decidability Results

Decidability Results

Theorem

The synthesis problem over singleton architectures is decidable for regular specifications.

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Theorem

The distributed synthesis problem over strongly connected architectures is decidable for AlocTL specifications.

Decidability Results

Theorem

The synthesis problem over singleton architectures is decidable for regular specifications.

Theorem

The distributed synthesis problem over strongly connected architectures is decidable for AlocTL specifications.

Proof

By reduction to the singleton case.

Note that we do not need to change the specification since it is closed under extension

Strongly connected architectures (2)

Proposition

If there are communication sets $\Sigma_{i,j}$ for $(i, j) \in E$ and a winning distributed strategy on the strongly connected architecture, then there is a winning strategy on the singleton.

Proof

Easy.

Strongly connected architectures

Proposition

If there is a winning strategy f over the singleton architecture then one can define internal signals sets and a distributed winning strategy for the strongly connected architecture.

Strongly connected architectures

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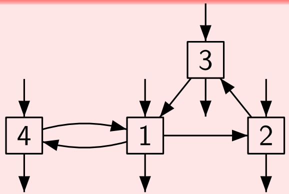
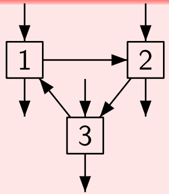




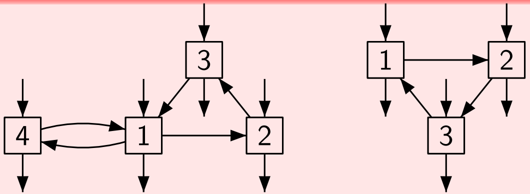
- We select a master process and a cycle.

Strongly connected architectures

Proposition

If there is a winning strategy f over the singleton architecture then one can define internal signals sets and a distributed winning strategy for the strongly connected architecture.

Proof



- We select a master process and a cycle.
- The master process will centralize information in order to simulate f and tell other processes which value to output

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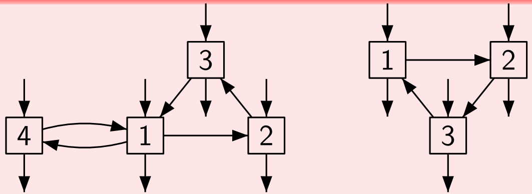


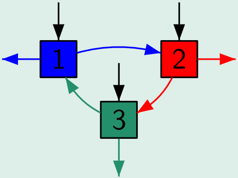
- We select a master process and a cycle.
- The master process will centralize information in order to simulate f and tell other processes which value to output
- Aim: create a run that will be a weakening of some f-run over the singleton

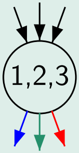
Centralize information

Example

Specification: $\mathrm{req}_3 \rightarrow \mathsf{F}_{32}(\neg\, \mathsf{Y}_2\, \mathrm{alert} \leftrightarrow \mathrm{grant})$

Strategy for the singleton: $f(\sigma) = \mathrm{grant}$ iff σ contains req_3 but no alert





Master collect information by sending a signal Msg through the cycle

t: 1, 2, 3

t':

Centralize information

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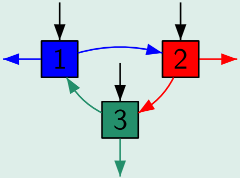

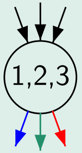

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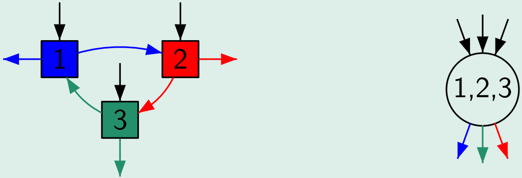

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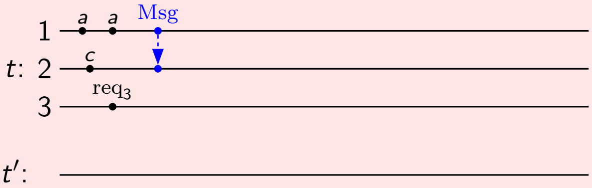

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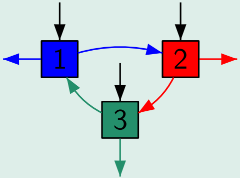

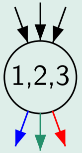

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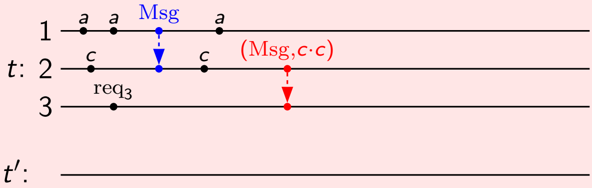

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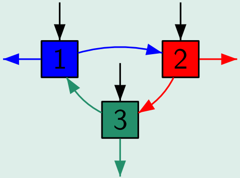

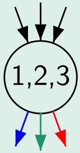

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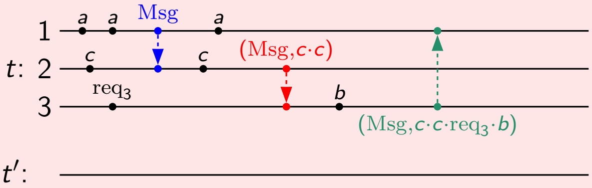

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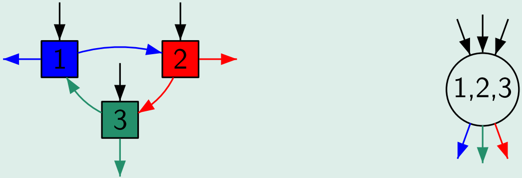

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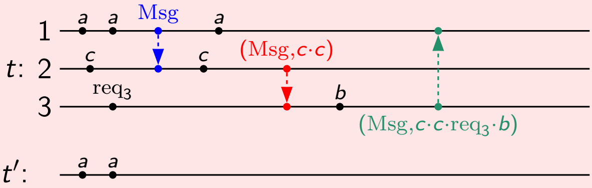

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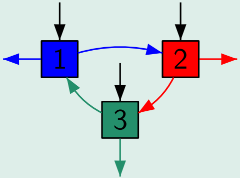

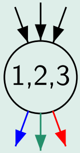

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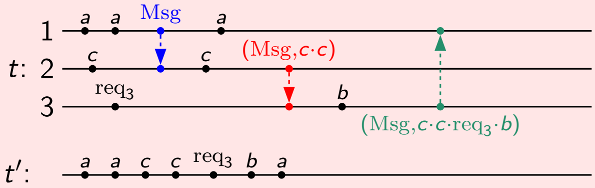

Tell processes what to output

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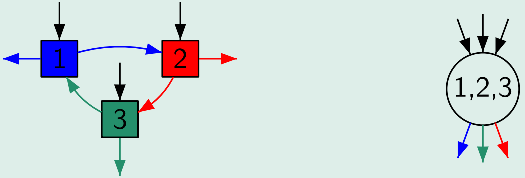
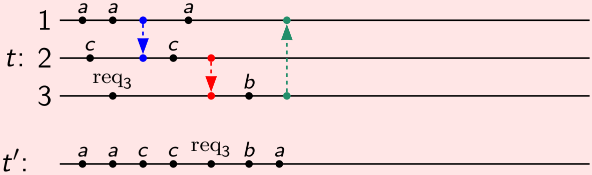


Master sends orders to other processes to simulate the strategy f



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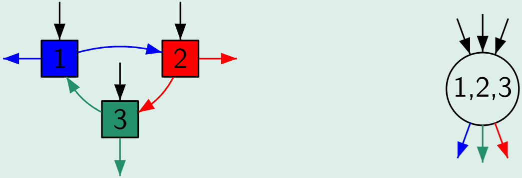

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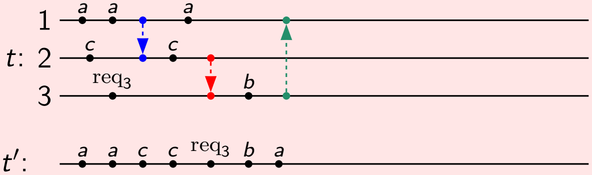

f : grant

Tell processes what to output

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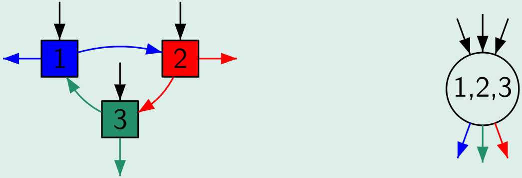

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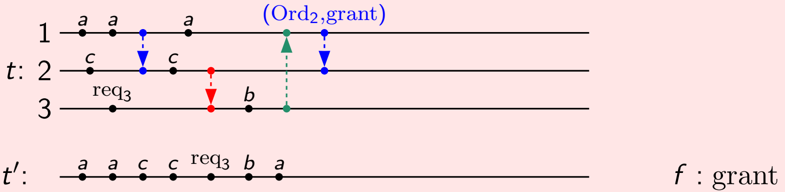
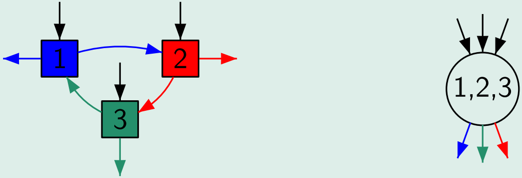


Tell processes what to output

Example

Specification: $\mathrm{req}_3 \rightarrow \mathsf{F}_{32}(\neg\, \mathsf{Y}_2\, \mathrm{alert} \leftrightarrow \mathrm{grant})$

Strategy for the singleton: $f(\sigma) = \mathrm{grant}$ iff σ contains req_3 but no alert



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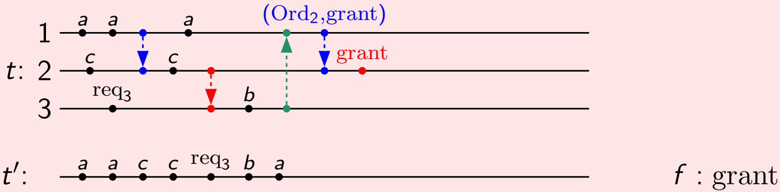

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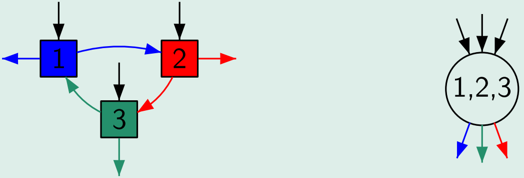

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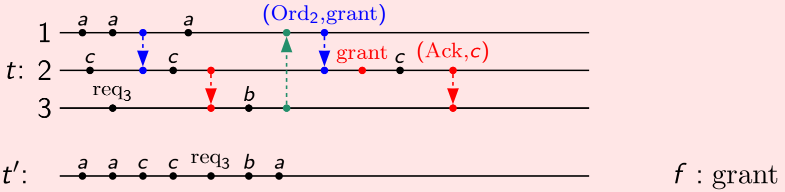

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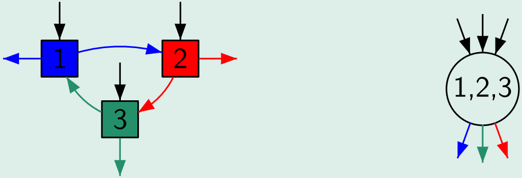

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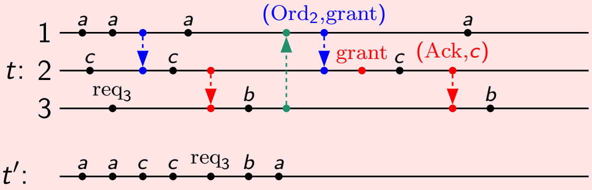

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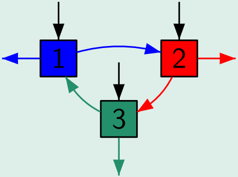

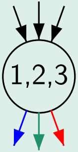

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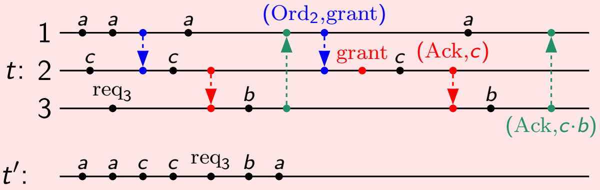

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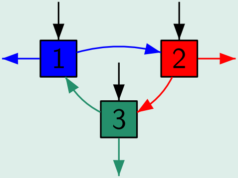

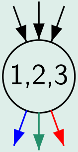

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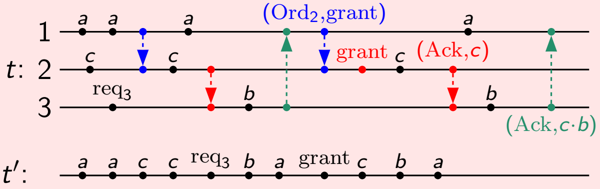

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Tell processes what to ouptut (2)

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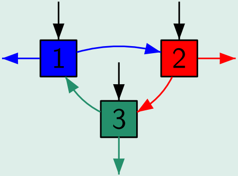

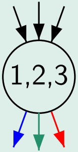

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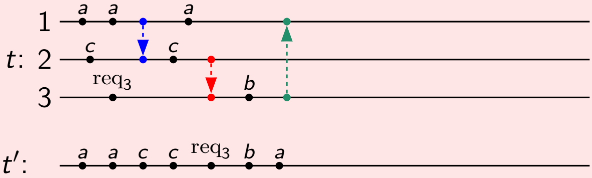

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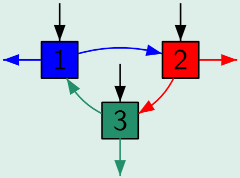

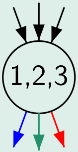

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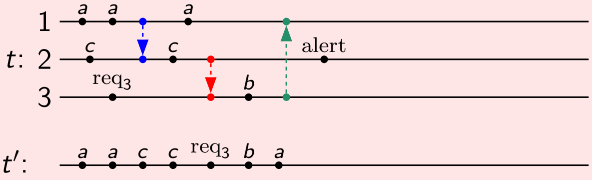

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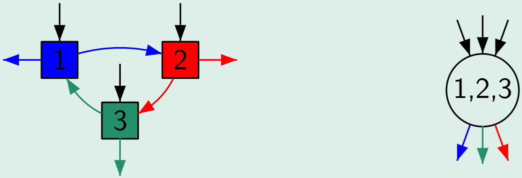

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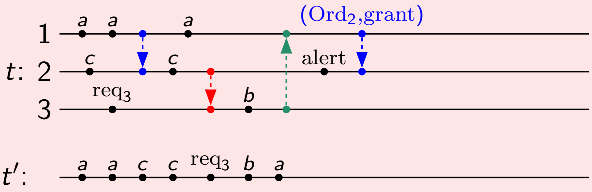

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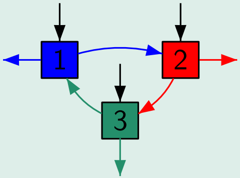

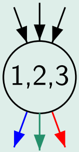

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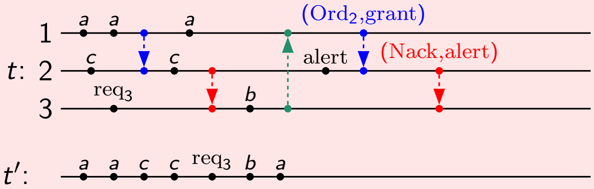

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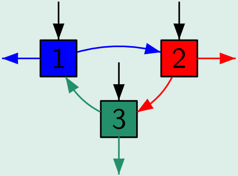

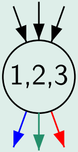

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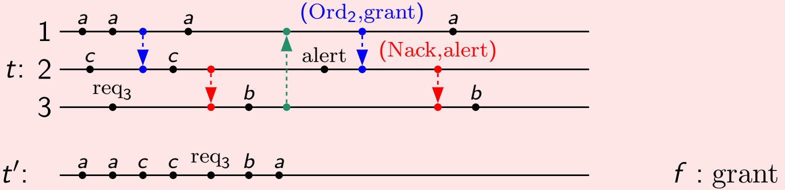

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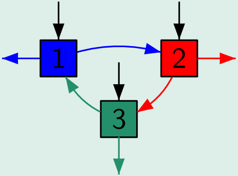

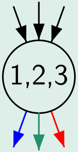

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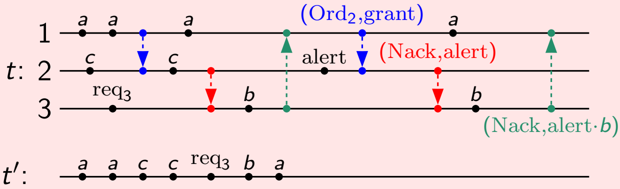

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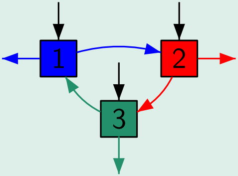

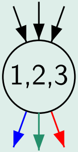

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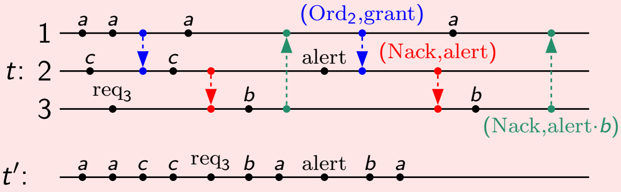

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Conclusion

Then $t' \models \varphi$ and, by closure property $\pi_\Gamma(t) \models \varphi$.

Memory

Proposition

If the strategy f over the singleton has finite memory, then we can distribute the strategy for the strongly connected architecture using

- finite alphabets $\Sigma_{i,j}$
- local strategies with finite memories

Conclusion

- Asynchrony removes undecidability causes
- We have defined a new model of communication
- We have identified a class of decidable architectures
- Hopefully, many more to come!