How to get decidability of distributed synthesis?

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Outline

1. Introduction
2. Model
3. Specification
4. Decidability Results
Synthesis of a reactive system

Two problems

- Decide whether there exists a program st. $P \parallel E \models \varphi, \forall E$.
- Synthesis: If so, compute such a program.

For reasonable systems and specifications, the problems are decidable.
Distributed synthesis

Two problems

1. Decide the existence of a distributed program such that their joint behavior $P_1 || P_2 || P_3 || P_4 || E$ satisfies $\varphi$, for all $E$.
2. Synthesis: If it exists, compute such a distributed program.
Distributed synthesis: Undecidable in general!? 

Synchronous semantics: Introduced by Pnueli Rosner ’90

- At each tick of a global clock, all processes and the environment output their new value.
- Undecidable with global specifications.
- Undecidable with constraints on internal channels.
- Undecidable with bandwidth constraints.
- Decidable for some architectures, e.g., pipelines.
Asynchronous semantics

P.G., Benjamin Lerman, Marc Zeitoun

- Behaviors are Mazurkiewicz traces
- Players = controllable actions
- Causal memory
- Specification: regular over Mazurkiewicz traces

Theorem

Synthesis problem is decidable for co-graph dependence alphabets, i.e., for series-parallel systems.
Asynchronous semantics

Our model

- Processes evolve asynchronously for local actions (i.e., communications with the environment)
- They can synchronize by signals = common actions initiated by only one process. A process cannot refuse reception of a signal.
- Specifications:
  - over partial orders
  - will not restrain communication abilities
Theorem

Synthesis problem is decidable for

- strongly-connected architectures,
- disjoint unions of decidable architectures.
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The model

Architectures

- Communication graph \((Proc, E)\)
- For each process \(i\), sets \(\text{In}_i\) and \(\text{Out}_i\) of input and output signals:
  \[ \Gamma = \bigcup_{i \in Proc} \text{In}_i \cup \bigcup_{i \in Proc} \text{Out}_i \]
- Processes choose sets \(\Sigma_{i,j}\) for \((i, j) \in E\)
- \[ \Sigma = \Gamma \cup \bigcup_{(i,j) \in E} \Sigma_{i,j} \]
- For each process \(i\),
  \[ \Sigma^c_i = \text{Out}_i \cup \bigcup_{(j, (i,j)) \in E} \Sigma_{i,j} \] is the set of signals it can send (control),
  \[ \Sigma_i = \text{In}_i \cup \Sigma^c_i \] is its alphabet.
A run is a Mazurkiewicz trace $t = (V, \lambda, \leq)$ over $(\Sigma, D)$ where $a \leq D b$ if there is a process that takes part both in $a$ and $b$. 
The model: strategies

Strategies

- Strategies are partial functions $f_i : \Sigma_i^* \rightarrow \Sigma_i^c$ with local memory.
- Signal semantics implies reactivity of processes to events.

Diagram:

1. $a$ -- $b'$
2. $a'$ -- $a'$
3. $f_1 : g$
4. $f_2 : h$
5. $f_3 : d$
The model: strategies

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- Signal semantics implies reactivity of processes to events.
- A run respects a strategy $f = (f_i)_{i \in \text{Proc}}$ (is an $f$-run) if each event of process $i$ labelled with a controllable action respects the strategy $f_i$.
- A run $t = (V, \lambda, \leq)$ is $f$-maximal if for each process $i$ either $V_i = \lambda^{-1}(\Sigma_i)$ is infinite, or $f_i$ is undefined on the maximal event of $V_i$. 

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**Strategies**

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![Diagram](image-url)
The model

Observable runs

Given a run $t = (V, \lambda, \leq)$, we define the observable run by

$$\pi_{\Gamma}(t) = (\Gamma, \lambda|_{\Gamma}, \leq \cap (\Gamma \times \Gamma))$$

where

$$\Gamma = \bigcup_{i \in \text{Proc}} \text{In}_i \cup \bigcup_{i \in \text{Proc}} \text{Out}_i$$
The synthesis problem

Given
- \( A = (\text{Proc}, E, \Gamma) \)
- \( \varphi \) a specification over \( \Gamma \)-labelled partial orders (observable runs)

Do there exist
- sets \( \Sigma_{i,j} \) for each \( (i,j) \in E \)
- and strategies \( f_i : \Sigma_i^* \rightarrow \Sigma_i^C \) for each \( i \in \text{Proc} \)

such that every \( f \)-maximal \( f \)-run \( t \) is such that \( \pi_{\Gamma}(t) \models \varphi \)?

If so, compute them
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Specifications

Communication induces order relation

1
2
3

1
2
3

1
2
3

1
2
3
Communication induces order relation
Specifications

Communication induces order relation

\[
\begin{array}{c}
\text{1} \\
\text{2} \\
\text{3}
\end{array}
\]

\[
\begin{array}{c}
a \\
b \\
c
\end{array}
\]
Specifications

Restrictions on specifications
- Specifications should not discriminate between a partial order and its order extensions
Specifications

Input events are not controllable by processes
Input events are not controllable by processes

Specifications
Specifications

Restrictions on specifications

- Specifications should not discriminate between a partial order and its order extensions
- Specifications should not discriminate between a partial order and its "weakenings"
Example of a logic closed by extension and weakening

**AlocTL**

\[ \varphi ::= a \mid \neg a \mid \varphi \lor \varphi \mid \varphi \land \varphi \]

\[ \mid X_i \varphi \mid \varphi U_i \varphi \mid \neg X_i \top \mid \varphi \tilde{U}_i \varphi \]

\[ \mid Y_i \varphi \mid \varphi S_i \varphi \mid \neg Y_i \top \mid \varphi \tilde{S}_i \varphi \]

\[ \mid F_{i,j}(\text{Out} \land \varphi) \mid \text{Out} \land H_{i,j} \varphi \]

with \( a \in \Gamma \) and \( i, j \in \text{Proc} \)
Example of a logic closed by extension and weakening

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Example of a logic closed by extension and weakening

### AlocTL

\[ \varphi ::= a \mid \neg a \mid \varphi \lor \varphi \mid \varphi \land \varphi \]

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\[ \mid Y_i \varphi \mid \varphi S_i \varphi \mid \neg Y_i \top \mid \varphi \tilde{S}_i \varphi \]

\[ \mid F_{i,j}(Out \land \varphi) \mid Out \land H_{i,j} \varphi \]

with \( a \in \Gamma \) and \( i, j \in \text{Proc} \)

### Formulae

- \( G_1(\text{request} \rightarrow F_{1,2}(Out \land grant)) \)
- \( G_2(\text{grant} \rightarrow (Out \land H_{2,1} \text{request})) \)

### Theorem

AlocTL is closed under extension and weakening
Closure by extension

¬F_{i,j} \varphi \text{ forbidden!}

\[ a \land \neg F_{1,2} b \]

\begin{align*}
1 & \quad a \\
2 & \quad b \\
\end{align*}

OK

\begin{align*}
1 & \quad a \\
2 & \quad b \\
\end{align*}

KO
Closure by extension

- $\neg F_{i,j} \varphi$ forbidden!
- $X_{i,j} \varphi$ forbidden!

```
a \wedge X_{1,2} c
```

OK

KO
Closure by extension

- $\neg F_{i,j} \varphi$ forbidden!
- $X_{i,j} \varphi$ forbidden!

Specification is not allowed to require concurrency

Closure by weakening

Ensured by $F_{i,j} \land \text{Out}$ and $\text{Out} \land H_{i,j} \varphi$. 
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Decidability Results

Theorem
The synthesis problem over singleton architectures is decidable for regular specifications.

Theorem
The distributed synthesis problem over strongly connected architectures is decidable for AlocTL specifications.

Proof
By reduction to the singleton case.
Note that we do not need to change the specification since it is closed under extension.
Proposition

If there are communication sets $\Sigma_{i,j}$ for $(i,j) \in E$ and a winning distributed strategy on the strongly connected architecture, then there is a winning strategy on the singleton.

Proof

Easy.
**Proposition**

If there is a winning strategy \( f \) over the singleton architecture then one can define internal signals sets and a distributed winning strategy for the strongly connected architecture.

**Proof**

- We select a master process and a cycle.
- The master process will centralize information in order to simulate \( f \) and tell other processes which value to output.
- Aim: create a run that will be a *weakening* of some \( f \)-run over the singleton.
Centralize information

Example

Specification: \( \text{req}_3 \rightarrow F_{32}(\neg Y_2 \text{ alert} \leftrightarrow \text{grant}) \)

Strategy for the singleton: \( f(\sigma) = \text{grant} \) iff \( \sigma \) contains \( \text{req}_3 \) but no alert

Master collect information by sending a signal \( \text{Msg} \) through the cycle

\[
\begin{align*}
\text{t: } 1 & \quad a \quad a \quad \text{Msg} \quad a \\
2 & \quad c \quad \downarrow \quad c \quad (\text{Msg}, c \cdot c) \\
\text{req}_3 & \quad (\text{Msg}, c \cdot c \cdot \text{req}_3 \cdot b) \\
3 & \quad b \quad \downarrow \quad b \\
\text{t': } & \quad a \quad a \quad c \quad c \quad \text{req}_3 \quad b \quad a
\end{align*}
\]
Tell processes what to output

Example

Specification: \( \text{req}_3 \rightarrow F_{32} (\neg Y_2 \text{alert} \leftrightarrow \text{grant}) \)

Strategy for the singleton: \( f(\sigma) = \text{grant} \) iff \( \sigma \) contains \( \text{req}_3 \) but no alert

Master sends orders to other processes to simulate the strategy \( f \)

\[ t: \begin{align*}
1 & \quad a \quad a \quad a \\
2 & \quad c \quad i \quad c \quad \text{(Ord}_2,\text{grant)} \quad \text{grant} \quad c \quad \text{(Ack},c) \\
3 & \quad \text{req}_3 \quad b \quad b \quad \text{Ack},c \cdot b
\end{align*} \]

\[ t': \begin{align*}
1 & \quad a \quad a \quad c \quad \text{req}_3 \quad b \quad a \quad \text{grant} \quad c \quad b \quad a \\
\end{align*} \]

\( f: \text{grant} \)
Tell processes what to output (2)

Example

Specification: \( \text{req}_3 \rightarrow F_{32}(\neg Y_2 \text{ alert} \leftrightarrow \text{grant}) \)
Strategy for the singleton: \( f(\sigma) = \text{grant} \) iff \( \sigma \) contains \( \text{req}_3 \) but no alert

Master sends orders to other processes to simulate the strategy \( f \)

\[
\begin{array}{l}
\text{t:} & 1 & a & a & a & (\text{Ord}_2, \text{grant}) & a & a \\
& c & c & & & \text{alert} & & (\text{Nack}, \text{alert}) \\
\text{req}_3 & b & & & & & b \\
\text{t\text{'}:} & a & a & c & c & \text{req}_3 & b & a & \text{alert} & b & a \\
\end{array}
\]
Lemma

$t'$ is an extension of $\pi_\Gamma(t)$.

Lemma

If $x <' y$ in $t'$ and $x \parallel y$ in $\pi_\Gamma(t)$ then $\lambda(y) \in \text{In}$.

Corollary

$\pi_\Gamma(t)$ is a weakening of $t'$.

Lemma

$t'$ is an $f$-maximal $f$-run.

Conclusion

Then $t' \models \varphi$ and, by closure property $\pi_\Gamma(t) \models \varphi$. 
If the strategy $f$ over the singleton has finite memory, then we can distribute the strategy for the strongly connected architecture using

- finite alphabets $\Sigma_{i,j}$
- local strategies with finite memories
Conclusion

- Asynchrony removes undecidability causes
- We have defined a new model of communication
- We have identified a class of decidable architectures
- Hopefully, many more to come!