An Introduction to Timed Systems

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Outline

Time!

Context: verification of embedded critical systems

Time

- naturally appears in real systems
- appears in properties (for ex. bounded response time)

➜ Need of models and specification languages integrating timing aspects

Adding timing informations

- **Untimed case:** sequence of observable events
  a: send message b: receive message

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$$(a, d_1)\ (b, d_2)\ (a, d_3)\ (b, d_4)\ (a, d_5)\ (b, d_6)\ \cdots$$

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d_2: date at which the first b occurs, ...

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    Ex: $(a, 1)(b, 3)(c, 4)(a, 6)$

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    Ex: $(a, 1)(b, 3)(c, 4)(a, 6)$
  - **Dense-time semantics:** dates are *e.g.* taken in $\mathbb{Q}_+$, or in $\mathbb{R}_+$
    Ex: $(a, 1.28).(b, 3.1).(c, 3.98)(a, 6.13)$

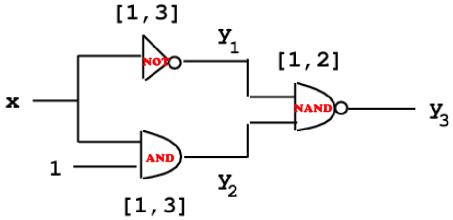
A case for dense-time

Time domain: discrete (*e.g.* $\mathbb{N}$) or dense (*e.g.* $\mathbb{Q}_+$ or $\mathbb{R}_+$)

- A compositionality problem with discrete time
- Dense-time is a more general model than discrete time
- But, can we not always discretize?

A digital circuit [Alur 91]

Discussion in the context of reachability problems for asynchronous digital circuits [Brzozowski, Seger 1991]



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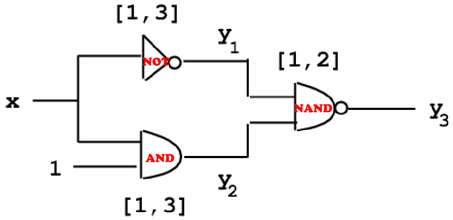

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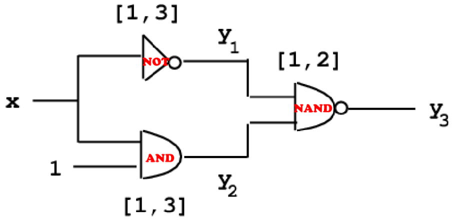

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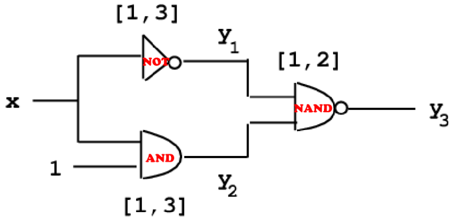

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However, many possible behaviours, e.g.

$$[101] \xrightarrow[1.2]{y_2} [111] \xrightarrow[2.5]{y_3} [110] \xrightarrow[2.8]{y_1} [010] \xrightarrow[4.5]{y_3} [011]$$

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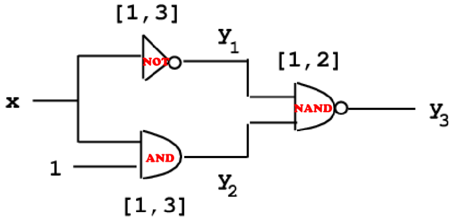

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Reachable configurations: {[101], [111], [110], [010], [011], [001]}

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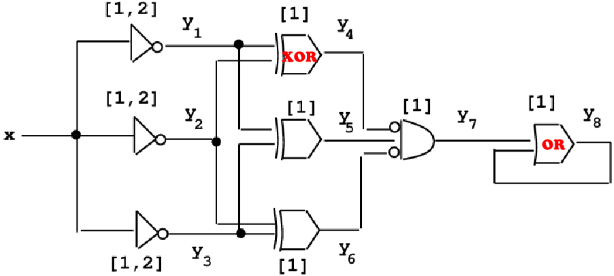

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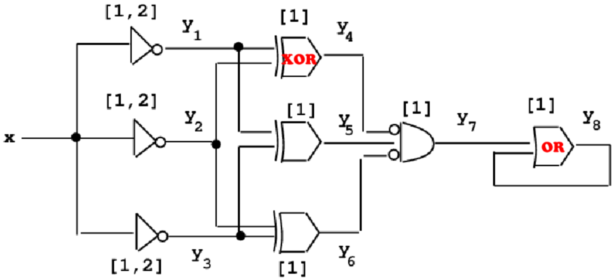

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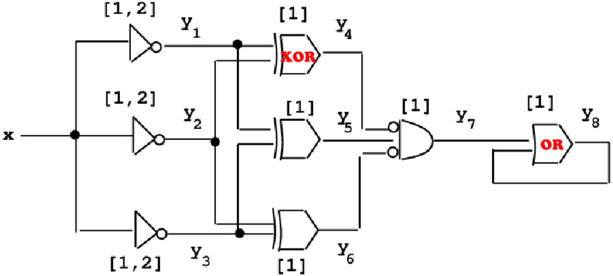

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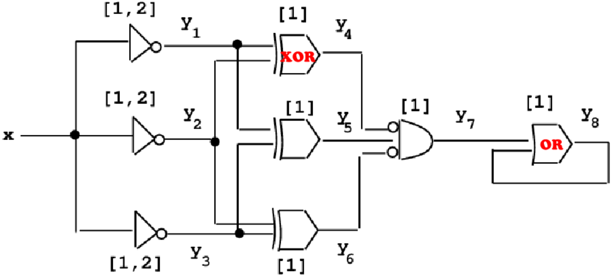

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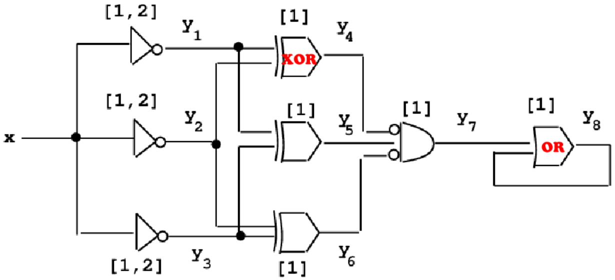

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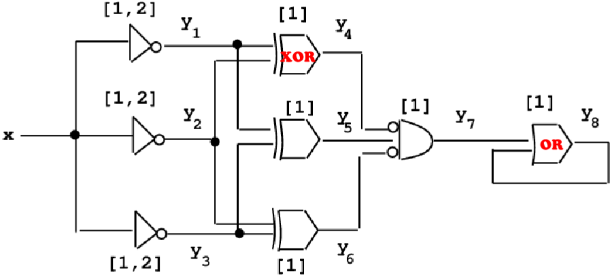

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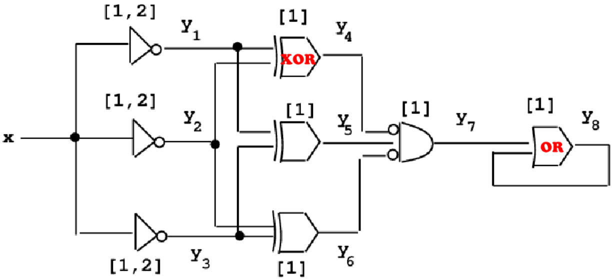

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Theorem [Brzozowski Seger 1991]

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Further counter-example

There exist systems for which no granularity exists. (see later)

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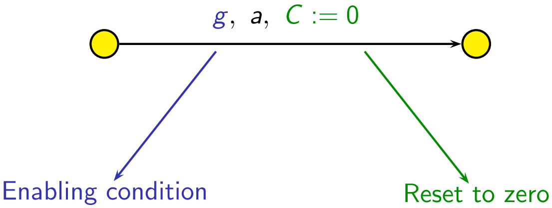
Hence, we better consider a dense-time domain!

Outline

Timed automata

[Alur,Dill 1990]

- A finite control structure + variables (clocks)
- A transition is of the form:



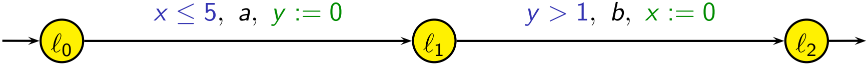
- An enabling condition (or guard) is:

$$g \quad ::= \quad x \sim c \quad | \quad g \wedge g$$

where $\sim \in \{<, \leq, =, \geq, >\}$

Timed automata (example)

x, y : clocks



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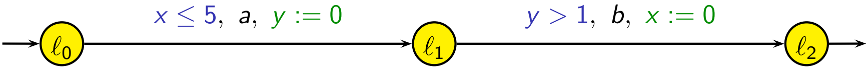

$$
\begin{array}{cccccccccc}
 & \ell_0 & \xrightarrow{\delta(4.1)} & \ell_0 & \xrightarrow{a} & \ell_1 & \xrightarrow{\delta(1.4)} & \ell_1 & \xrightarrow{b} & \ell_2 \\
x & 0 & & 4.1 & & 4.1 & & 5.5 & & 0 \\
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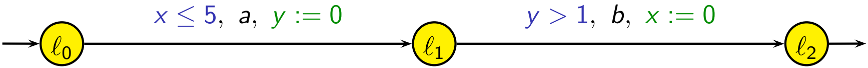

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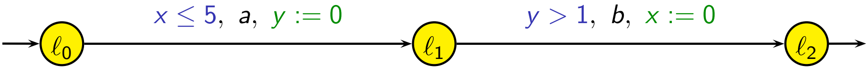

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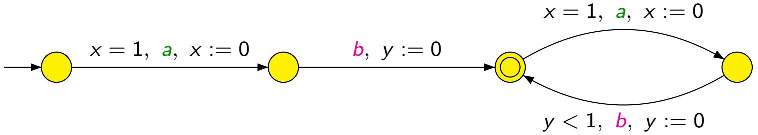
(clock) valuation

➜ timed word $(a, 4.1)(b, 5.5)$

Timed automata semantics

- $\mathcal{A} = (\Sigma, L, X, \longrightarrow)$ is a TA
- **Configurations:** $(\ell, v) \in L \times T^X$ where T is the time domain
- **Timed Transition System:**
  - **action transition**: $(\ell, v) \xrightarrow{a} (\ell', v')$ if $\exists \ell \xrightarrow{g,a,r} \ell' \in \mathcal{A}$ s.t. $\begin{cases} v \models g \\ v' = v[r \leftarrow 0] \end{cases}$
  - **delay transition**: $(\ell, v) \xrightarrow{\delta(d)} (\ell, v + d)$ if $d \in T$

Discrete *vs* dense-time semantics



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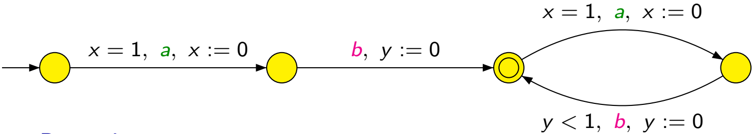

- Dense-time:
  $L_{dense} = \{((ab)^\omega, \tau) \mid \forall i,\ \tau_{2i-1} = i \text{ and } \tau_{2i} - \tau_{2i-1} > \tau_{2i+2} - \tau_{2i+1}\}$

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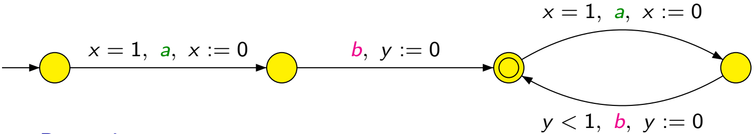

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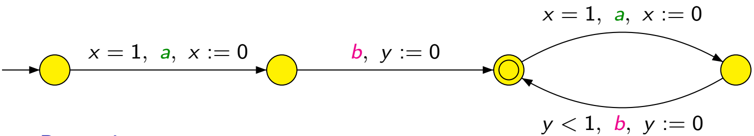

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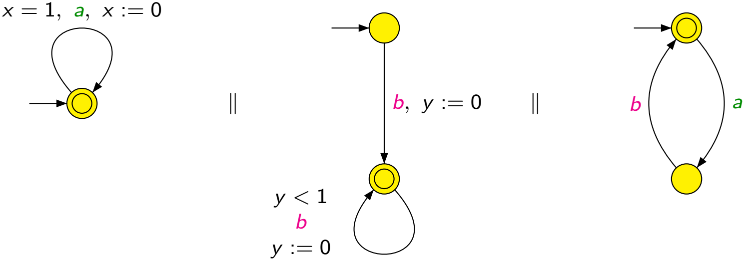
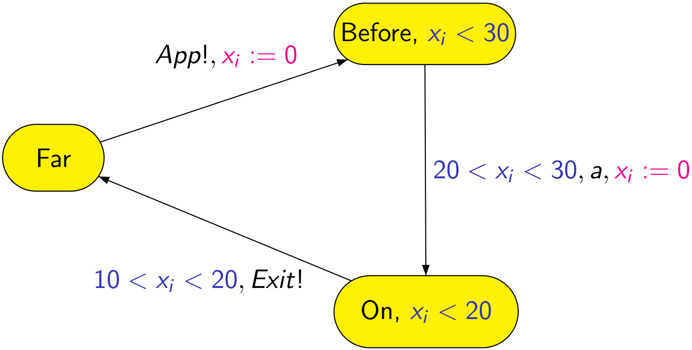


Classical verification problems

- reachability of a control state
- $\mathcal{S} \sim \mathcal{S}'$: bisimulation, etc...
- $L(\mathcal{S}) \subseteq L(\mathcal{S}')$: language inclusion
- $\mathcal{S} \models \varphi$ for some formula φ: model-checking
- $\mathcal{S} \parallel A_T$ + reachability: testing automata
- ...

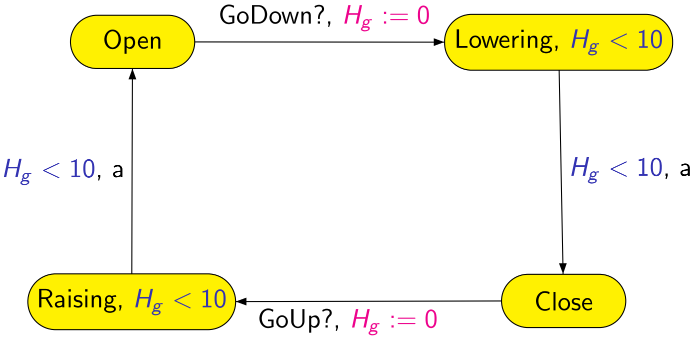
The train crossing example (1)

Train$_i$ **with** $i = 1, 2, \ldots$



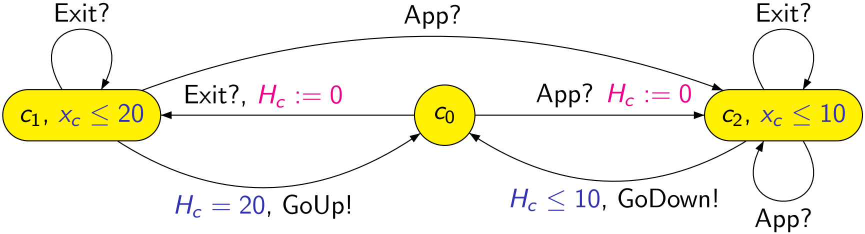
The train crossing example (2)

The gate:



The train crossing example (3)

The controller:



The train crossing example (4)

We use the synchronization function f:

Train_1	Train_2	Gate	Controller	
$App!$	.	.	$App?$	App
.	$App!$	.	$App?$	App
$Exit!$	.	.	$Exit?$	$Exit$
.	$Exit!$	.	$Exit?$	$Exit$
a	.	.	.	a
.	a	.	.	a
.	.	a	.	a
.	.	$GoUp?$	$GoUp!$	$GoUp$
.	.	$GoDown?$	$GoDown!$	$GoDown$

to define the parallel composition $(\mathsf{Train}_1 \parallel \mathsf{Train}_2 \parallel \mathsf{Gate} \parallel \mathsf{Controller})$

NB: the parallel composition does not add expressive power!

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Some properties one could check:

- Is the gate closed when a train crosses the road?

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$$\neg\mathbf{EF}(\text{gate.Close} \wedge \mathbf{E}(\text{gate.Close}\ \mathbf{U}_{>5\ \text{min}}\ \neg\text{gate.Close}))$$

Outline

Verification

Emptiness problem: is the language accepted by a timed automaton empty?

- reachability properties (final states)
- basic liveness properties (Büchi (or other) conditions)

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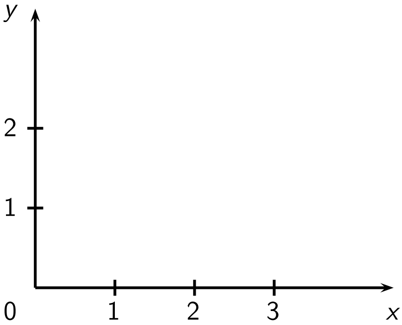
Method: construct a finite abstraction

The region abstraction



Equivalence of finite index

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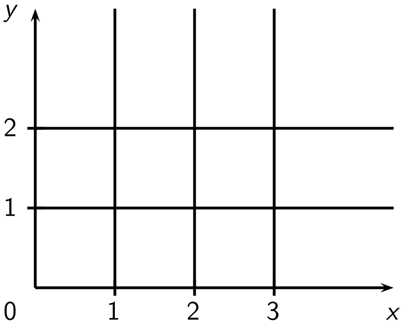

Equivalence of finite index

- "compatibility" between regions and constraints

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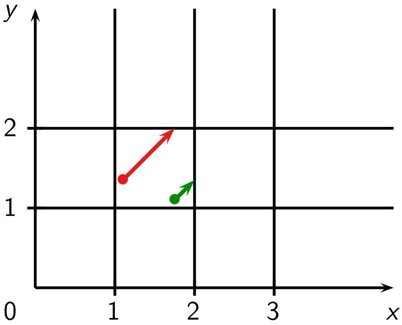

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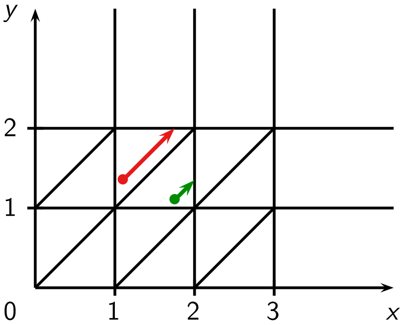

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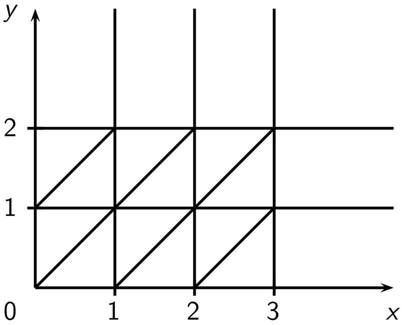

Equivalence of finite index

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➜ a time-abstract bisimulation property

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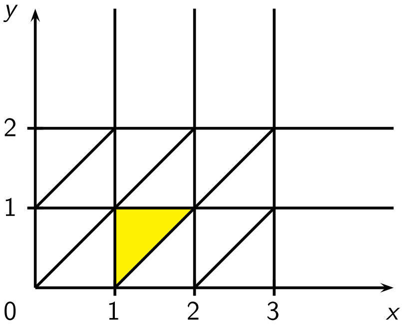

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region defined by
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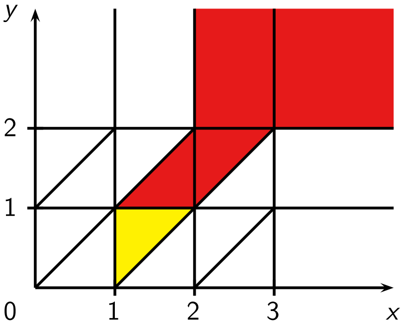

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successor regions

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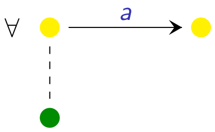
Time-abstract bisimulation



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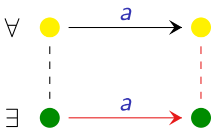

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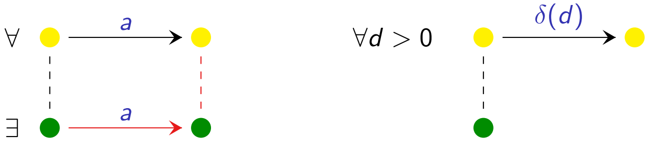
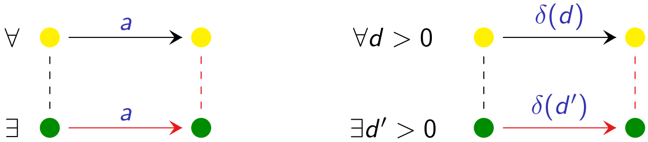


Time-abstract bisimulation

$$\begin{tikzcd} \forall & \bullet \arrow[r, "a"] \arrow[d, dash, dashed] & \bullet \arrow[d, dash, dashed] \\ \exists & \bullet \arrow[r, "a"] & \bullet \end{tikzcd}$$

$$\begin{tikzcd} \forall d > 0 & \bullet \arrow[r, "\delta(d)"] \arrow[d, dash, dashed] & \bullet \arrow[d, dash, dashed] \\ \exists d' > 0 & \bullet \arrow[r, "\delta(d')"] & \bullet \end{tikzcd}$$

Time-abstract bisimulation



$$(\ell_0, v_0) \xrightarrow{a_1, t_1} (\ell_1, v_1) \xrightarrow{a_2, t_2} (\ell_2, v_2) \xrightarrow{a_3, t_3} \ldots$$

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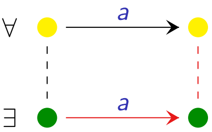

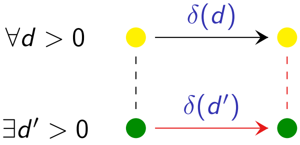

$$\begin{tikzcd}
(\ell_0, v_0) \arrow[r, "a_1, t_1"] \arrow[d] & (\ell_1, v_1) \arrow[r, "a_2, t_2"] \arrow[d] & (\ell_2, v_2) \arrow[r, "a_3, t_3"] \arrow[d] & \ldots \\
(\ell_0, R_0) \arrow[r, "a_1"] & (\ell_1, R_1) \arrow[r, "a_2"] & (\ell_2, R_2) \arrow[r, "a_3"] & \ldots
\end{tikzcd}$$

with $v_i \in R_i$ for all i.

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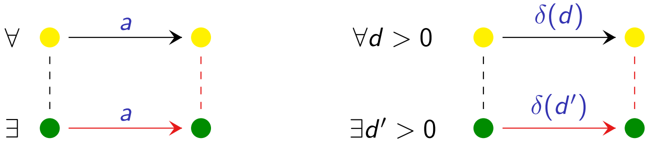

$$
\begin{tikzcd}
(\ell_0, v_0) \arrow[r, "a_1, t_1"] \arrow[d, leftrightarrow] & (\ell_1, v_1) \arrow[r, "a_2, t_2"] \arrow[d, leftrightarrow] & (\ell_2, v_2) \arrow[r, "a_3, t_3"] \arrow[d, leftrightarrow] & \dots \\
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Region automaton $\equiv$ finite bisimulation quotient

timed automaton $\bigotimes$ region abstraction

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$\ell \xrightarrow{g,a,C:=0} \ell'$ is transformed into:

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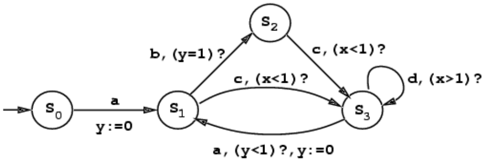
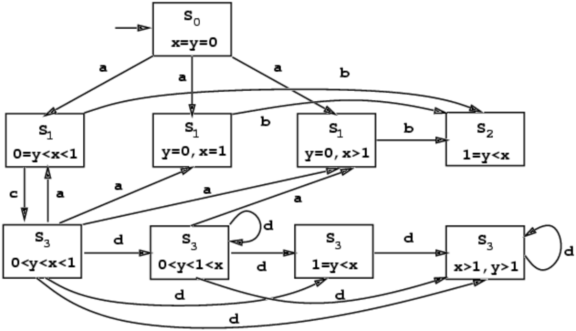
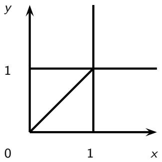
$\mathcal{L}$**(reg. aut.) = UNTIME(**$\mathcal{L}$**(timed aut.))**

where $\mathrm{UNTIME}((a_1, t_1)(a_2, t_2)\dots) = a_1 a_2 \dots$

An example [AD 90's]







Consequence of region automata construction

Region automata:

correct finite (and exponential) abstraction for checking reachability/Büchi-like properties.

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However...

everything can not be reduced to finite automata...

A model not far from undecidability

Some bad news...

- Language universality is undecidable **[Alur,Dill 1990]**
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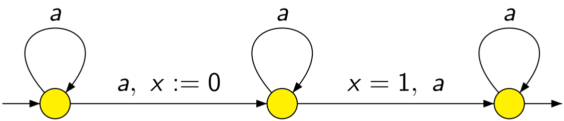
An example of non-determinizable/non-complementable timed aut.:



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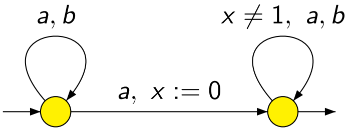

UNTIME $\left(\overline{L} \cap \{(a^* b^*, \tau) \mid \text{all } a's \text{ happen before 1 and no two } a's \text{ simultaneously}\}\right)$ is not regular **(exercise!)**

Partial conclusion

- This idea of a finite bisimulation quotient has been applied to many "timed" or "hybrid" systems:
  - various extensions of timed automata
    [Bérard,Diekert,Gastin,Petit 1998] [Choffrut,Goldwurm 2000] [Bouyer,Dufourd,Fleury,Petit 2004] $\cdots$

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- Note that in practice, the region automaton is not constructed, and symbolic technics based on *zones* are used

Outline

The example of alternating timed automata

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[Lasota,Walukiewicz 2005,2007] [Ouaknine,Worrell 2005,2007]

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Example

"No two a's are separated by 1 unit of time"

$$\begin{cases} \ell_0, a, \mathit{true} & \mapsto \quad \ell_0 \wedge (x := 0, \ell_1) \\ \ell_1, a, x \neq 1 & \mapsto \quad \ell_1 \\ \ell_1, a, x = 1 & \mapsto \quad \ell_2 \\ \ell_2, a, \mathit{true} & \mapsto \quad \ell_2 \end{cases}$$

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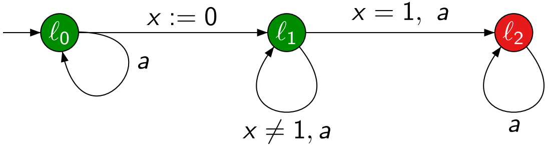

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- Emptiness of ATA is undecidable.
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Lower bound: simulation of a lossy channel system... [Schnoebelen 2002]

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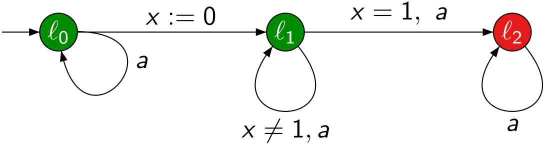

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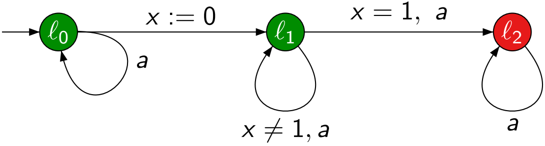

Execution over timed word $(a, .3)(a, .8)(a, 1.4)(a, 1.8)(a, 2)$

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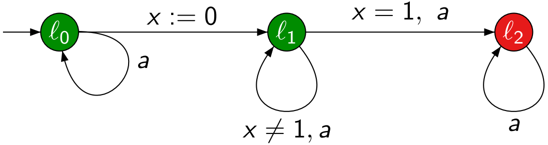

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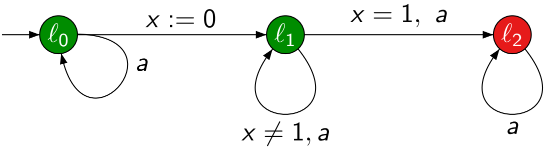

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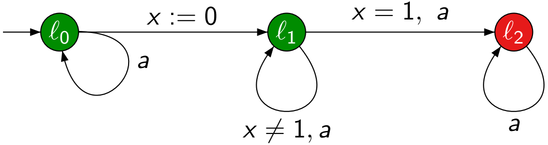

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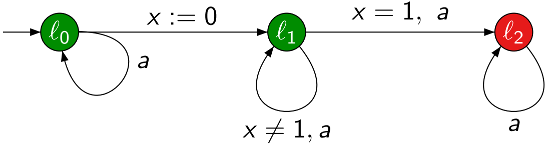

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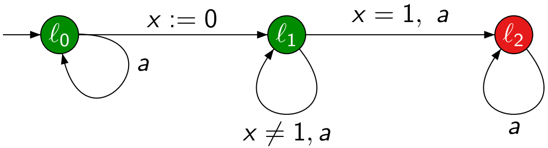

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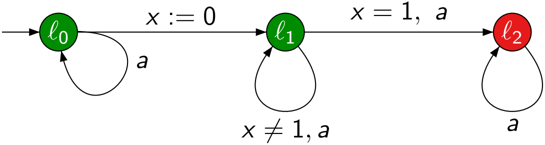

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An abstraction

A configuration $=$ a finite set of pairs (ℓ, x)

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0.0

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0.0 0.2

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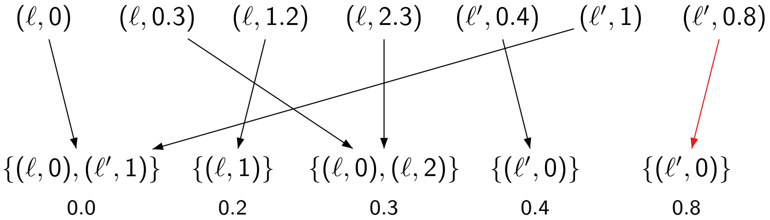

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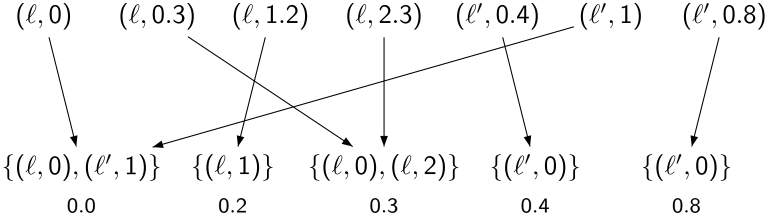
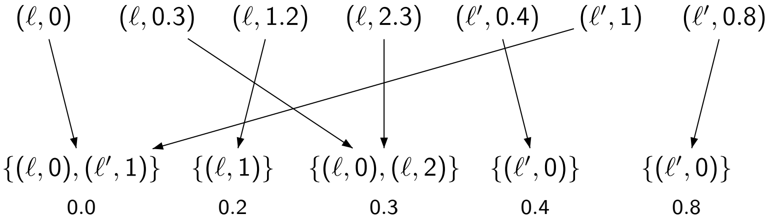


An abstraction

A configuration = a finite set of pairs (ℓ, x)



Abstracted into: $\{(\ell, 0), (\ell', 1)\} \cdot \{(\ell, 1)\} \cdot \{(\ell, 0), (\ell, 2)\} \cdot \{(\ell', 0)\} \cdot \{(\ell', 0)\}$

Abstract transition system

$\boxed{\{(\ell, 0), (\ell', 1)\}} \cdot \boxed{\{(\ell, 1)\}} \cdot \boxed{\{(\ell, 0), (\ell, 2)\}} \cdot \boxed{\{(\ell', 0)\}} \cdot \boxed{\{(\ell', 0)\}}$

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Time successors:

Abstract transition system

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Time successors:

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Transition $\ell \xrightarrow{x>2, x:=0} \ell''$:

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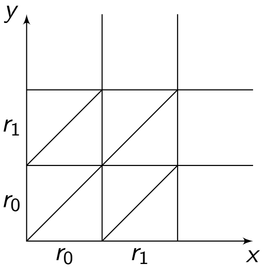
Alternative

The abstract transition system can be simulated by a kind of FIFO channel machine.

A digression on timed automata



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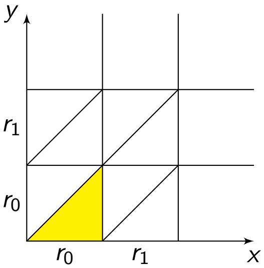

$x, y \in r_0$, $\{y\} < \{x\}$

$\boxed{(y, r_0)} \cdot \boxed{(x, r_0)}$

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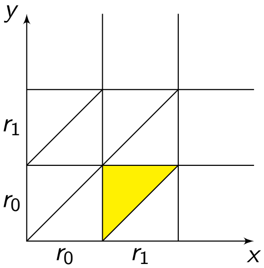

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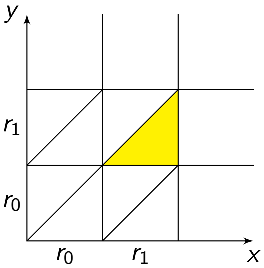

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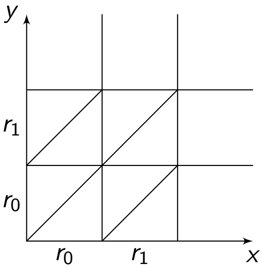

The classical region automaton can be simulated by a channel machine (with a single bounded channel).

Partial conclusion

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- networks of single-clock timed automata **[Abdulla,Jonsson 1998]**

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Some current streams of research in timed systems:

- quantitative model-checking
- real-time logics
- robustness, implementability issues
- timed games
- ...