Use of a full wave correct-by-design command to control a multilevel modular converter

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«MMC», «Full wave control»

Abstract

This paper proposes a method to synthesize a full wave control applied to a multilevel modular converter (MMC). This method guarantees the output waveform and the balancing of the capacitors. Numerical simulations and experiments are used to check the validity of the approach.

Introduction

Multilevel Modular Converter (MMC) is a voltage source converter (VSC) based high voltage direct current (HVDC) [1]. It is more and more used to interconnect grids for example the interconnection between Spain and France or interconnection between Pittsburg and San Francisco (Trans Bay – USA). It also used in renewable energies for grid connection of large offshore wind farm for example the BorWin1 project in the North Sea [2].

The MMC consists in the association of several switching cells associated with a capacitor. The control strategy must ensure both the multilevel output waveform and the balancing of the capacitors. The most used strategy currently to drive the switching cells consists in using a pulse width modulation with PI controllers [3-6].

In this paper, we propose a full wave control. The balancing of the voltages across the capacitors is ensured thanks to the redundancy of the combinations that allows the correct output level. The full wave control reduces the number of switching and thus reduces the switching losses of the converter.

In the next parts, the full wave control is detailed in the case of a 3-levels MMC and generalized for a high number of levels.

Full wave control of a MMC converter

Principle of the control

In this part, the full wave control of a 3-levels MMC is detailed. In our example, the MCC is used as a single-phase midpoint inverter. Four switching cells compose this basic structure and the DC voltage source is split into two identical voltages $U_0/2$ thus realizing the midpoint (Fig. 1-a). This midpoint is used to simplify the study but a second half bridge MMC can replace it. The multilevel output voltage

of the MMC is noted U. In Fig. 1-b a simplify structure is represented where capacitors are replace by ideal voltage sources U_c .



Fig. 1: 3-levels MMC converter. (a) Real structure. (b) Idealized structure

The switches functions that drive the switching cells are noted com_{T-i} and com_{B-i} ; where i is the index of a switching cell (the index u and l are used to the upper and lower parts of the converter). The voltages across the capacitor take the same value noted U_{C} . The output voltages of the switching cells are noted U_{T-i} and U_{B-i} . The relation between the output voltages and the switching functions is given by (1).

$$U_{k-i} = (1 - com_{k-i}) U_c$$
 (1)

where k is $\{T \text{ or } B\}$ and $\{i\}$ is the index a switchning cell

The summation of the whole of the output voltages must be equal to the voltage of the DC-bus (2).

$$U_{T-1} + U_{T-2} + U_{B-1} + U_{B-2} = U_0$$
(2)

Because the switching functions are binaries (can take the value 0 or 1) the relation given by (3) must be respected.

$$com_{T-1} + com_{T-2} + com_{B-1} + com_{B-2} = 4 - \frac{U_0}{U_1}$$
where the quantity $\left[4 - \frac{U_0}{U_1}\right]$ must be an integer
(3)

Thus, the voltage across the capacitors can take three possible values:

τī

$$1 - U_{C} = \frac{U_{0}}{3} \implies \operatorname{com}_{T-1} + \operatorname{com}_{T-2} + \operatorname{com}_{B-1} + \operatorname{com}_{B-2} = 1$$

$$2 - U_{C} = \frac{U_{0}}{2} \implies \operatorname{com}_{T-1} + \operatorname{com}_{T-2} + \operatorname{com}_{B-1} + \operatorname{com}_{B-2} = 2$$

$$3 - U_{C} = U_{0} \implies \operatorname{com}_{T-1} + \operatorname{com}_{T-2} + \operatorname{com}_{B-1} + \operatorname{com}_{B-2} = 3$$

In cases 1 and 3, the summation of the switching functions is equal to 1 and 3 respectively that implies only two possible levels on the output voltage U. However, in case 2, the summation is equal to 2 that

allows to obtain three possible levels on U. Those combinations and the corresponding output waveform are represented on Fig. 2.



Fig. 2: (a) Patterns allowing to obtain a 3-levels output waveform represented in (b).

It can be noticed that four different combinations allow to obtain the state B. This redundancy will be used to balance the voltage across the capacitors. For example, if $i_T > 0$ and $Uc_{T-1} < Uc_{T-2}$, the state B *a* or *b* can be applied to charge de capacitor C_1 .

Based on this principle, the command strategy of the upper part of the structure can be resumed by the synoptic represented in Fig. 3. This command strategy allows to reduce switchings compared to classical controls using a PWM and thus allows to reduce switching losses.



Fig. 3: Full wave control strategy of a 3-levels MMC.

Generalization of the full wave control

Controller

In our approach, the top and the bottom parts of the MMC half bridge are controlled separately. If the charge of any capacitor would be maintained exactly at a value of U_0/n , the system would behave perfectly. Therefore, our goal is to maintain the capacitor voltages close to this value as possible. Our controller relies on the following observations:

- when the current flowing trough the top or bottom part of the half bridge is non negative, going trough one of the capacitors will charge it,

- when the current is non positive, going trough a capacitor will discharge it.

Therefore, we will use the time when the current is positive to charge all the capacitors that are discharged with respect to the optimal value of U_0/n . If no capacitor voltage is lower than this value, we will charge the capacitors least charged to try to maintain the capacitor voltages as close as possible to the optimal value. In a same manner, we will use the time where the current is negative to discharge the most charged capacitors.

Assuming that k cells needs to be used in order to obtain the desired level of output, our algorithm works in the following way:

- when called, it will sort all the capacitor from the least charged to the most charged.

- each capacitor will obtain a number between 1 and n, where 1 means the capacitor is the least charged, and n the most charged

- if the current is positive, all the cells corresponding to capacitors with a number less or equal to k will be used in order to charge the corresponding capacitors,

- if the current is negative, all the cells corresponding to capacitors with a number greater than to n-k will be used in order to discharge the corresponding capacitors,

Remark: the current is only measured at the beginning of the call. It is possible that right after the measure, the current switches sign and the computed control will produce the opposite of what was desired. However, in practice, the behavior of the current is regular enough so that even if this issue occurred, it will be quickly recovered.

The code of our controller is presented in Fig. 6 in pseudocode, where *Order* is the function that assign a number between 1 and n to each capacitor where 1 means the capacitor is the least charged, and n the most charged.



Fig. 4: Algorithm of a n-levels MMC.

Simulation

Using Plecs [7], we have simulated a MMC and its controller with n = 120 cells, $C = 4700 \ \mu\text{F}$ and l = 1mH. In Fig.7 (a) (resp. (b)), we present the evolution of each voltage capacitor in the upper (resp. lower) part of the half bridge.

It is difficult to distinguish between the voltages of each capacitor because of the way our controller works. Indeed, it is easy to see that our controller ensures that the charges of all the capacitors remain close to each other. In Fig. 9, the output voltage and its Fourier spectrum are represented. This simulation allows to conclude that the implemented algorithm ensures both the balancing of the

voltage capacitor and the output waveform.

Remark: the algorithm proposed in this paper is specific of the MMC architecture. An algorithm that can work on any architecture [8-9] has been designed and tested on several flying-capacitor converters examples [10]. The main drawback of the general algorithm is its exponential complexity while the one proposed in this paper can be implemented in O(n.log(n)). This low complexity allows an on the fly-computation even for large number of cells.



Fig. 8: Voltage across the capacitors in the top (a), and the bottom (b) of the MMC half bridge.



Fig. 9: Output voltage (a) and the its Fourier spectrum (b).

Experimental validation

In order to validate the algorithm, a 7-levels half bridge MMC converter was realized (Fig. 10) such as the one represented in Fig 1-a. It is composed by 6 switching cells both for the top and the bottom part of the structure. The DC voltage U_0 is equal to 200 V, the capacitors C are equal to 470 μ F and the inductances l are equal to 2 mH. An inductive load L equal to 600 mH composes the output load. The control is ensure thanks to a DSP TMS320F28335 from Texas Instrument and computerized in Matlab Simulink. The control strategy is the one represented on Fig. 6 with n = 6. In order to transform the desired input sine waveform to a quantized waveform (represented by the variable k is Fig. 6), a block diagram represented in Fig. 10 is used. The sine wave has maximum amplitude of 1 and the quantization interval is equal to 1/3. This solution will be discussed later.



Fig.10: Experimental setup; a 7-levels MMC converter.



Fig.10: Quantization of the input sine waveform.

The waveforms of the output voltage and load current are represented in Fig. 11 - a. This figure show that the output voltage waveform is conformed to the one expected. The load current has a quasi-sine waveform due to the low harmonic content of the voltage (Fig. 11 - b).



Fig.11: Experimental output waveforms (a) and spectrum of the output voltage (b).

In order to check the balancing of the voltage across the capacitors, three voltages was measured and represented in Fig. 12. We can observed that the balancing in ensure and the voltage is on average equal to 33 V ($U_0/6$). The variation is equal to about 10 V and is depending on the value of the capacitors. This variation can be reduced if the value of the capacitors is increased.



Fig.12: Measurement of the voltage across three different capacitors.

This implementation validates the control strategy used. Moreover, in order to use this converter, magnitude of the output voltage must be adjustable. This point will be discussed in the next part.

Adjustment of the magnitude of the output voltage

In our setup, the magnitude of the output voltage can be adjusted using the input sine voltage (Fig.10). However, if all the levels are exploited, the variation of the input sine wave is limited. The extreme variations of the output voltage were simulated and represented in Fig. 13 as well as the associated spectrums. The magnitude of the fundamental voltage can only varies from 80% to 100%. Moreover, the decrease of the fundamental generates an increase of harmonics.



Fig.13: Extreme values of the output voltage using a quantized sine wave: waveforms (a) and associated spectrums (b).

To keep the lowest level of harmonics, it is possible to calculate durations of each level is order to eliminate harmonics 5 and 7 (for example) and to ensure the maximum variation of the output voltage. The simulation for a 9-levels waveform is represented in Fig. 14 as well as the associated spectrum. In this case, the magnitude of the fundamental voltage can only varies from 53% to 120% and the harmonics level is kept low. In the case of a high number of levels, durations can be calculated to keep the THD (Total Harmonic Distortion) as low as possible.



Fig.14: Extreme values of the output voltage using calculated durations: waveforms (a) and associated spectrums (b).

Conclusion

In this paper, a full wave control method is proposed. This method, applying to a MMC converter, allows to both ensure the multilevel output voltage waveform and the correct balancing of the voltage capacitors. This kind of control has been also validated in flying-capacitors converters. The full wave control should increase the efficiency of the structure but this point has still to be demonstrated.

In the future, the developed MMC converter will be tested when it is connected to the grid. The control of the amplitude of the voltage will be also tested and validated and the impact on the current harmonics will be studied.

References

[1] A. Lesnicar, R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range", Power Tech Conference Proceedings, 2003 IEEE Bologna

[2] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, et M. Prats, "The age of multilevel converters arrives," Industrial Electronics Magazine, IEEE, vol. 2, n°. 2, p. 28-39, 2008.

[3] J. Barrena, L. Marroyo, M. Vidal, et J. Apraiz, "Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM," Industrial Electronics, IEEE Transactions on, vol. 55, n°. 1, p. 21-29, 2008.

[4] C. Schauder et H. Mehta, "Vector analysis and control of advanced static VAr compensators," Generation, Transmission and Distribution, IEE Proceedings C, vol. 140, n°. 4, p. 299-306, 1993.

[5] L. Gyugyi, "Application characteristics of converter-based FACTS controllers," in Power System Technology, 2000. Proceedings. PowerCon 2000. International Conference on, vol. 1, p. 391-396 vol.1, 2000.

[6] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," in Power Electronics Conference (IPEC), 2010 International, p. 508-515, 2010.

[7] Plecs Website http://www.plexim.com

[8] A. Girard, G. Pola, et P. Tabuada, "Approximately Bisimilar Symbolic Models for Incrementally Stable Switched Systems," Automatic Control, IEEE Transactions on, vol. 55, n°. 1, p. 116-126, 2010.

[9] P. Fraigniaud, D. Ilcinkas, S. Rajsbaum, et S. Tixeuil, "The Reduced Automata Technique for Graph Exploration Space Lower Bounds," in Theoretical Computer Science, vol. 3895, O. Goldreich, A. Rosenberg, et A. Selman, Éd. Springer Berlin / Heidelberg, 2006, p. 1-26.

[10] G. Feld, L. Fribourg, D. Labrousse, S. Lefebvre, B. Revol and R. Soulat. Control of Multilevel Power Converters using Formal Methods. Research Report LSV-12-14, Laboratoire Spécification et Vérification, ENS Cachan, France, June 2012. 14 pages.