# Distributed and Coupled Electrothermal Model of Power Semiconductor Devices

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**ABSTRACT**

Electro-thermal model of power semiconductor devices are of key importance in order to optimize their thermal design and increase their reliability. The development of such an electro-thermal model for power MOSFET transistors (COOLMOS$^{TM}$) based on the coupling between two computation softwares (Matlab and Cast3M) is described in the paper. The elaborated 2D electro-thermal model is able to predict i) the temperature distribution on chip surface well as in volume, ii) the effect of the temperature on the distribution of the current flowing within the die and iii) the effects of the ageing of the metallization layer on the current density and the temperature. In the paper, the used electrical and thermal models are described as well as the implemented coupling scheme.

***Index Terms—*** Electro-thermal model, Power semiconductor transistors, Ageing of power semiconductor devices, Short circuit, Degradation of the metallization layer.

## 1.INTRODUCTION

The development of electronic components and circuits, as power semiconductor modules in applications with a high level of current and / or voltage, continually faces many technological challenges. Particularly, the temperature increase arising from the dissipation of power semiconductor devices remains one of the major obstacles to large-scale integration and reliability.

Power semiconductor modules integrate different types of material (electrical conductors, insulators, semiconductors) with different coefficient of thermal expansion (CTE). The effects of power cycling due to mission profiles result in temperature variations in the packaging. The resulting thermo-mechanical constraints are responsible for the major failure modes of these devices, thus compromising the operation and safety of complex systems (automotive, aeronautics, space). These devices may also suffer of extremely hard working operations, resulting from an accident in the case of short-circuit conditions depending on the application circuit and its environment. During these modes of operation, the device is in the on-state, the supply voltage is applied between Drain and Source and the current is only limited by the saturation of the transistor. It results for these modes of operation a very high dissipation of power in the dies and therefore a very fast increase of the temperature which can lead to immediate failure depending on short-circuit duration. Thus, short-circuit operations are among of the various modes of operation of power semiconductor modules responsible for the most severe thermal stresses.

Insofar as these constraints are sufficiently short (low level of dissipated energy), the devices are able to undergo many of them though not without consequences on their remaining lifespan. So, it is of the first importance to carry out investigations on the behavior of power devices under such severe repetitive working operations. Fig. 1 shows waveforms of a short circuit applied to a 800V COOLMOS$^{TM}$ transistor resulting for a dissipated energy equal to 5,95 J/cm$^2$.

Especially, in order to be able to predetermine how many short-circuit pulses a given device is able to undergo before failure for given operating conditions, it is necessary to point out ageing effects and indicators of failure on the devices and the associated failure mechanisms.

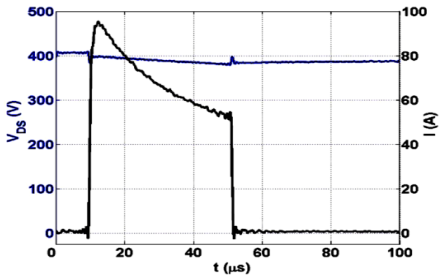



**Fig.1:** Short circuit waveforms in the case of a dissipated energy equal to 5,95 J /cm$^2$ (E = 400V, $T_C$ = 25°C), 800V COOLMOS$^{TM}$

Previous studies have shown a significant degradation of the metallization layer during ageing (aluminum reconstruction) which results in a significant increase of the aluminum sheet resistance. Fig. 2 summarizes the evolution of the relative Al metallization resistance during the repetition of the short circuit operations in test conditions with different dissipated energies [1].

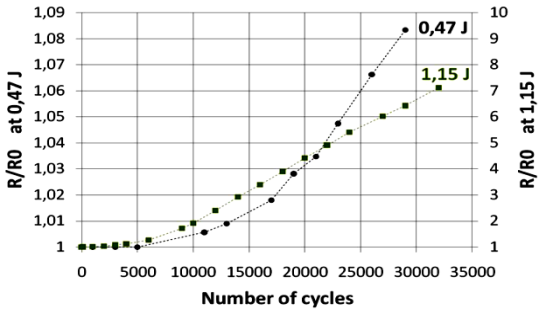



**Fig. 2:** Increase of Al. resistance during ageing [1].

Consequently, electro-thermal simulation becomes very important to evaluate the temperature distribution in the die. These models are also essential to assess the risk of electrical or thermal instability especially in transient operations. These models are well developed to help designers to improve both technological and design parameters [2-5].

Two main approaches can be used for the coupling of electrical and thermal models for the electro-thermal modeling of power semiconductor devices: relaxation and direct methods [6].

This paper describes an electro-thermal model for which thermal and electrical problems are treated separately by two different simulators (MATLAB-SIMULINK and CASTEM) in a, relaxation method framework. To achieve the electro-thermal coupling, a dedicated interface has been created in order to exchange temperatures and power dissipation sources information between the two different models.

## 2. ELECTROTHERMAL MODEL

### 2.1 Description of the implemented models

*2.1.1 Electrical model*

The tested component is a 800V COOLMOS$^{TM}$ transistor packaged by Microsemi [1]. Figure 3 depicts an example of electrical environment of such a device in the case of DC/DC conversion. The switching of the transistor is controlled by the gate to source voltage $v_{GS}$. The load of the circuit is assumed to be an ideal current source $I_0$ and the freewheeling diode is assumed to be also an ideal component (zero voltage in on-state, no recovery current). There are also basically two modes of operation for the transistor:

(a) if the transistor is in the off-state ($v_{GS} < v_{GSTH}$), then $v_{ds} = U_0$ and $i_d = 0$

(b) if the transistor is in the on-state, then $v_{ds} \approx 0$ and $i_d = I_0$ (conduction).

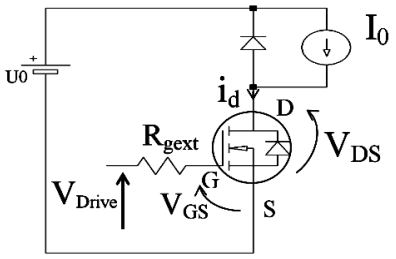



**Figure 3.** Buck chopper for the transient validation of the electro-thermal model

*2.1.2 Transistor geometry*

The 3-D geometry of the considered power module is shown in Figure 4. The module is composed of five layers of different materials: DBC (Copper, Alumina, and copper), solder between die and copper, Silicon and Aluminum metallization (metallization of the die). The gate which is distributed on the die is not shown in the figure; but the current in the silicon is controlled by the electric field in the silicon induced by gate to source voltage $V_{GS}$.

The dies are the main sources of losses in the power module (mainly on-state losses in the case of MOSFET transistors). Thus, they are subjected to the highest temperature excursions in operation. The metallization which is deposited on the upper surface of the chips will be submitted also in constraints of operation to the most severe thermal stresses encountered by the power module. In order to analyze the distribution of the temperature and the coupling with the current distribution in the die, the silicon layer is divided into *N* cells, each of

which will have its own current $I_n$ depending on the local temperature $T_n$ and the local gate to source voltage $v_{GSn}$ ($N = 4$ in this paper). In a first step, and for the sake of simplicity the temperature which is considered to influence the electrical performances is located at the top surface of the die, at the interface between silicon and aluminum.

The drain current in the transistor is flowing from the top copper layer of the DBC through the silicon, the aluminum layer to the bond wires. The distribution of the current in the aluminum layer will be also dependent on the bond wire location.

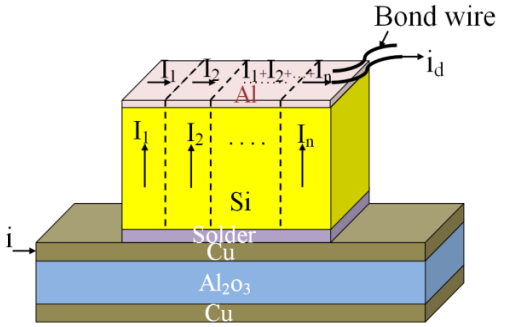



**Figure 4.** Power die divided in several cells soldered to a DBC substrate.

2.1.3 Transistor model

In a first approach, a simplified model of the transistor has been used. The current in each cell of the die is defined as follows:

$$i_d = \begin{cases} 0 \;\; if \;\; v_{gs} < v_{th} \\ K_p.\left(v_{ds}(v_{gs} - v_{th}) - \frac{v_{ds}^2}{2}\right) \;\; if \;\; \begin{bmatrix} v_{gs} \geq v_{th} \\ v_{ds} \geq v_{gs} - v_{th} \end{bmatrix} \\ \frac{K_p}{2}.(v_{gs} - v_{th})^2 \;\; if \;\; \begin{bmatrix} v_{gs} \geq v_{th} \\ v_{ds} \leq v_{gs} - v_{th} \end{bmatrix} \end{cases} \quad (1)$$

Where $v_{th}$ and $K_p$ are functions of the local temperature T as well as the carrier mobility.

$$v_{th\,(T)} = v_{th\,(T0)} - \varphi.(T - T0) \quad (2)$$

$$K_{p(T)} = \frac{\mu.c_{ox}.Z}{L.N} \quad (3)$$

$$\mu_{(T)} = \mu_0.\left(\frac{T}{T0}\right)^{-m} \quad (4)$$

The local current $I_n$ in each cell of the die depends on the global voltage $v_{dsn}$, the local gate to source voltage $v_{gsn}$ and the local temperature $T_n$. The drain current $i_d$ is the sum of these currents:

$$i_{dn} = i_d(v_{dsn}, v_{gsn}, T_n), \quad (5)$$

$$and \; i_d = \sum_{n=1}^{N} i_{dn}$$

The simplified electrical model of the transistor is shown in Figure 5.a and the equivalent circuit for $N$ cells is shown in figure 5.b. The gate voltage $V_{GS}$ is distributed over the $N$ partitions as voltage $v_{GSn}$. $R_{gext}$ is the gate drive resistance and $L_G$ the gate drive parasitic inductance. The gate resistance of polysilicon is distributed in each of the $N$ segments ($R_g$ for each cell). On-state losses and short circuit losses are assumed to be localized in the $N$- drift region. $C_{GS}$, $C_{DS}$ and $C_{DG}$ are also distributed on each segment. In order to simplify the model, these capacitances are considered in a first step as voltage independent.

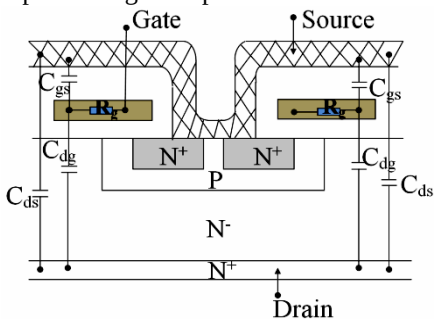



**Figure 5. a)** Simplified structure of a power MOSFET.

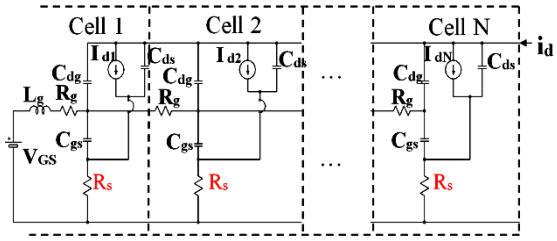



**Figure 5. b)** Distributed electrical model of the die.

**Table 1.** Device model parameters

| | |
|---|---|
| $T_0$ | 298 K |
| $V_{T0}$ | 3V |
| $\Phi$ | $8{,}5.10^{-3}$ $VK^{-1}$ |
| $\mu_0$ | 200 $cm^2V^{-1}s^{-1}$ |
| $C_{ox}$ | $1{,}05\times10^{-3}$ $Fm^{-1}$ |
| $M$ | 2,42 |
| $R_{gext}$ | 5 Ω |
| $R_g$ | 0.25 Ω |
| $L_g$ | $100.10^{-9}$ H |
| $C_{dg}$ | $15.10^{-12}$ F |
| $C_{ds}$ | $0{,}2825.10^{-9}$ F |
| $C_{gs}$ | $0{,}2975.10^{-9}$ F |
| $I_0$ | 10 A |
| $U_0$ | 400 V |

According to the different states of the transistor, two differential equations determine the behavior of the circuit.

In phase (a), $v_{ds}$ is fixed at $U_0$ while $i_d$ is depending on gate to source voltage. In phase (b), $i_d$ is fixed at $I_0$ and $v_{dsn}$ depends on local temperature and local gate to source voltages. In the following, we give the differential equations for each state for *N* cells,

$$\dot{x} = \boldsymbol{A_a}.x(t) + \boldsymbol{B_a}.u(t,y,T) \quad (6a)$$

$$\dot{x} = \boldsymbol{A_b}.x(t) + \boldsymbol{B_b}.u(t,y,T) \quad (6b)$$

$$y(t) = \boldsymbol{C_a}.x(t) + \boldsymbol{D_a}.u(t,y,T) \quad (7a)$$

$$y(t) = \boldsymbol{C_b}.x(t) + \boldsymbol{D_b}.u(t,y,T) \quad (7b)$$

$\mathbf{A_a}$, $\mathbf{A_b}$, $\mathbf{B_a}$, $\mathbf{B_b}$, $\mathbf{C_a}$, $\mathbf{C_b}$, $\mathbf{D_a}$ and $\mathbf{D_b}$ are the different matrix that describe the electrical equations of the system in states (a) and (b). The different blocks controlling the electric and thermal models were built in Matlab-Simulink as shown in the following figure.

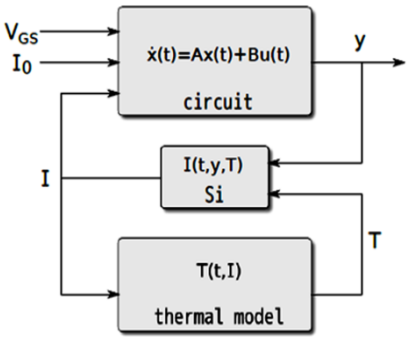



**Figure 6.** Control of the transistor model

## 2.2 Thermal model

### 2.2.1 Geometry

On the idealized geometry given in Figure 4, one can distinguish different materials. From the thermal point of view the component is a domain Ω (Fig. 7) which can be decomposed into 5 several sub-domains corresponding to the 5 used materials (Copper, Aluminum oxide, solder, Silicon, Aluminum), so that:

$$\Omega = \Omega_{cu}\, U\Omega_{Al2o3} U\Omega_{cu}\, U\, \Omega_{solder}\; U\Omega_{si}\, U\Omega_{Al} \quad (8)$$

### 2.2.2 Heat equations

The thermal problem is a classical transient heat problem submitted to fixed temperatures, fluxes, and sources linked to the currents and the voltages inside the component [7]. *T(x,t)* is the field of temperature defined on Ω x [0,$t_f$], where x denote the position and t the time. The final time of the study is denoted $t_f$.

The governing equations are defined in each subdomain:

$$\rho(x).c(x).\frac{\partial T(x,t)}{\partial t} - \lambda.\Delta\big(T(x,t)\big) = g(x,t) \quad (9)$$

Were $\rho(x)$, $c(x)$ and $\lambda$ are respectively the density, the specific heat and the thermal conductivity of each subdomain. Thermal parameters are considered temperature independent in a first step.

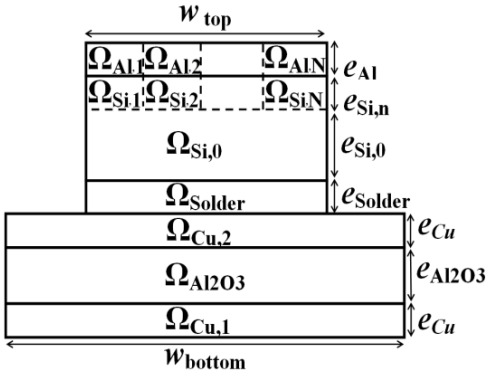



**Figure 7.** Domain decomposition for Ω.

**Table 2.** Thermal constants

| | |
|---|---|
| $\rho_{cu}$ | 8700 kg.m$^{-3}$ |
| $\rho_{Al2O3}$ | 3970 kg.m$^{-3}$ |
| $\rho_{solder}$ | 7360 kg.m$^{-3}$ |
| $\rho_S$ | 2330 kg.m$^{-3}$ |
| $\rho_{Al}$ | 2700 kg.m$^{-3}$ |
| $c_{Cu}$ | 385 J.kg$^{-1}$.K$^{-1}$ |
| $c_{Al2O3}$ | 780 J.kg$^{-1}$.K$^{-1}$ |
| $c_{sold}$ | 180 J.kg$^{-1}$.K$^{-1}$ |
| $c_{Si}$ | 700 J.kg$^{-1}$.K$^{-1}$ |
| $c_{Al}$ | 900 J.kg$^{-1}$.K$^{-1}$ |
| $kc_u$ | 400 W.m$^{-1}$.K$^{-1}$ |
| $k_{Al2}$ | 30 W.m$^{-1}$.K$^{-1}$ |
| $k$ | 55.5 W.m$^{-1}$.K$^{-1}$ |
| $k_{Si}$ | 148 W.m$^{-1}$.K$^{-1}$ |
| $k_{Al}$ | 160 W.m$^{-1}$.K$^{-1}$ |

**Table 3.** Geometrics parameters

| | |
|---|---|
| $e_{cu}$ | 200 µm |
| $e_{Al2O3}$ | 380 µm |
| $e_{solder}$ | 50 µm |
| $e_{Si,0}$ | 170 µm |
| $e_{Si,n}$ | 50 µm |
| $e_{Al}$ | 3 µm |
| $w_{bottom}$ | 5 cm |
| $w_{top}$ | 5,5 mm |

## 3. SIMULATION

### 3.1 Coupled simulation scheme

The above system has been implemented in Matlab-Simulink, while the thermal model of the transistor is implemented using the finite elements tool Cast3M™. The resolution of the electric model follows an explicit scheme, while the thermal model is in an implicit form. The coupled simulation will therefore be performed in an interleaved simulation scheme shown in Figure 8. In this figure, E refers to the electric simulation, while T relates to the thermal simulation. The two processes communicate via a first-in-first-out channel (FIFO).

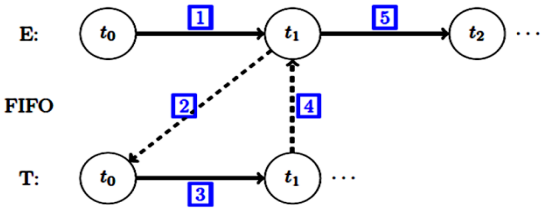



**Figure 8.** Interleaved simulation scheme

In the initial state (at $t_0$), all temperatures are assumed to be equal to $T_0$. The electric simulation performs one time step of length $\sigma$, while the thermal simulator is idle. Then (at $t_1$), the current values of $I_{dn}$ and $v_{dsn}$ are sent via the FIFO to the thermal simulator. With these values, the thermal simulation performs a step of $\sigma$ as well, reaching $t_1$, while the electric simulation remains in a waiting state. Having finished its computation, the thermal simulator sends the new temperatures $T_n$ to the electric model, completing the first step.

Note that in an explicit form, a very small $\sigma$ may be needed to guarantee the convergence of the electric simulation ($\sigma \approx 10^{-9}$ to $10^{-11}$ s during switching). On the other hand, the thermal effects take place on a much larger time-scale ($10^{-6}$ s to $10^{-3}$ s). Exchanging data after each $\sigma$ would be very expensive (time consuming 5 mn). Thus, the sampling time used to synchronize the simulators will not be identical to the internal time step for resolving the electric model. Instead, a variable time step solver is chosen within Simulink to guarantee the convergence at low cost, while the simulation processes are synchronized at a fixed sample time $\sigma_s$. Since under normal conditions, the temperatures change very slowly compared to the electric values, we expect that the error introduced by this approximation is negligible if $\sigma_s$ is chosen small enough.

## 4. RESULTS

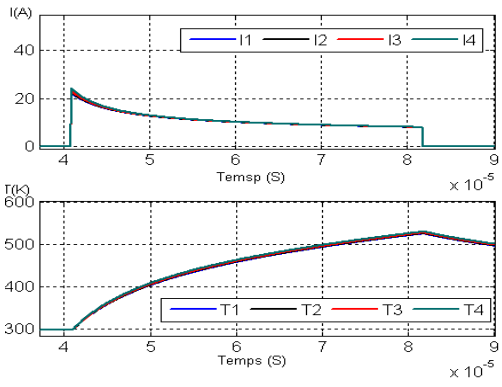
We have used the electro-thermal model presented in the first part of this paper in order to simulate the effect of short-circuit operations. In this extreme situation, the voltage $v_{ds}$ across the transistors remains equal to $U_0$ while the current controlled by Equation (1),

$i_d = \frac{K_p}{2}.(v_{gs} - v_{th})^2$ depends on the device characteristics and the temperature.

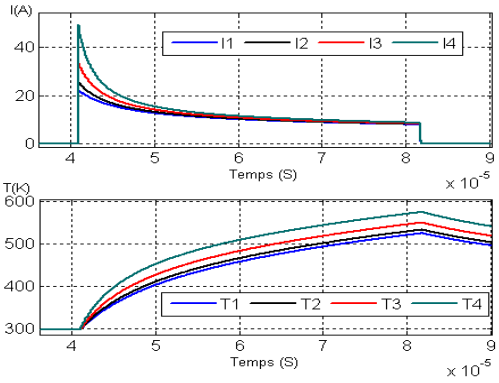
Large variations of temperature during these modes of operations make necessary the use of an electro-thermal model. The temperatures will rise quickly to significant high values, this in turn will influence the values of parameters $K$ and $v_{th}$.

Figure 9 shows the values of the four semiconductor currents in the distributed electro-thermal model and the respective maximum temperatures in the four cells in this extreme situation.

Electro-thermal effects are clearly visible in the reduction of the saturation current due to the temperature increase. In these conditions, with a low value of the aluminum sheet layer resistance, the effect of the distribution of the elementary cells is negligible.




**a)** Before aging




**b)** After aging

**Figure 9.** Current and temperature in short-circuit mode **a)** Before aging, **b)** After aging.

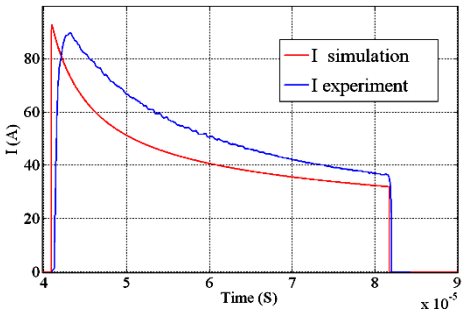



**Figure 10.** Current variation versus time obtained by simulation (red curve) and by measurement (blue curve).

A comparison between the drain current provided by the electro-thermal model and by measurement is presented in Figure 10. The heating effects on the drain current decrease are correctly described despite the excessive simplicity of the electrical model. This result allows to validate the electro-thermal model.

First results of aluminum ageing are also presented considering an increase of the aluminum resistivity by a factor of ten. Electro-thermal effects are visible as effects of cells distributions. These first results must be nevertheless analyzed in detail and compared to experimental results in a future work in order to better understand effect of aluminum degradation to failures.

## 5. CONCLUSION

We have described a novel simulation technique for performing electro-thermal simulations of power semiconductor devices. This new approach will allow us to finely analyze the current distribution in the chip. Moreover, it is found that this model can provide information on the physical origin of some failures.

In a future work, we plan to measure the surface temperature of the chips using an IR camera to validate the thermal calculations and the effect of metallization ageing on current distribution in the die.

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