VALMEM meeting (ANR project)



Meeting minutes 27/05/2010

Remy Chevallier 042/63/25 eSRAM team / Crolles1

1.Goal of the meeting

- Status on VALMEM project
- LIP6 : Temporal extraction integration (Pirouz/Patricia/Dominique)
- 3.2.LIP6: VHDL2TA: Automated translation of VDHL with timings into timed automaton format (HyTech/Uppaal) (Abdelrezzak/Emmanuelle)
- LSV: Parameterize model: IMITATOR2 (Etienne/Laurent)
- Publication status

2.Attendees

Emmanuelle Encrenaz	LIP6
Abdelrezzak Bara	LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

3.Summary of the meeting

3.1.LIP6: VHDL2TA: Automated translation of VDHL with timings into timed automaton format (HyTech/Uppaal)

- The access time (Taa) computed by this flow is providing boundaries embedding the values computed manually. However, the boundaries can be improved
- Based on automated algorithms, the boundaries have been improved:
 [253, 304] → [258, 298] (target is 276)

3.2.LIP6: Temporal extraction integration

- Automated timing computation performed
- The improvement of the flow should be based on the modeling of the constraints in complex gates which improve the performances: configuration used is improving the performances whereas the flow is modeling configuration which are not used and impacts the performances
- \rightarrow This flow should help VHDL2TA to improve the boundaries

3.3.LSV: Parameterize model: From IMITATOR to IMITATOR2

- IMITATOR2 is improving the performances a lot by using dynamic graph modeling. The simplified SPSMALL runs in 1 minute instead of 1hour and half.
- However, the full SPSMALL cannot be verified
- \rightarrow The next investigation is to replace the matrix constraints modeling approach by polyedra constraints modeling (targeting June)

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4.Actions

- Administrative
 - Follow-up the 'Accord de consortium' story (All) [asap]
- Provide by hands the timings expected by the new timing methodology (LIP6/Temporal extraction)
- Based on timing provided manually, compute the new boundaries (LIP6/VHDL2TA)
- IMITATOR2 improvement with polyedra constraint modeling (LSV)

5.Next meeting

The next meeting is planned in LIP6 at the end of June.

6.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	Done
D1.2	Build web site for the project	R	LIP6	0→6	Done
D1.3	Description of the conception flow	R	ST	6 → 12	Study 1 done
	applied on a study				Study 2 done
					Study 3 not started
					Run time of conception flow
					done
D2.1	State of art in memory verification	R	LIP6	0→6	Done
	methodologies				
D2.2	Definition of a new functional and	R	LIP6	0→6	Done
	timed model				
D2.3	Mixing of abstraction methods and	R	LIP6	6 → 12	Done
	temporal characterization				
D2.4	Abstraction tool prototype	Р	LIP6	12→48	ongoing
D3.1	Temporal automaton modeling	R	LSV	6 → 12	Done
	adapted to memory				
D3.2	Temporal automaton model checking	R	LSV	12 → 18	Done
	adapted to memory				
D3.3	verification tool prototype	Р	LSV	12→24	Done
D4.1	Description of the conception flow	R	ST	12→18	Not started
	applied on other studies				
D4.2	Experimentation of prototypes on	R & D	ST	18 → 48	ongoing
	real study			_	
D4.3	Comparison of results from current	R	ST	30→48	ongoing
	verification methods and new				
	methods				

The targets are described in months.

Delivery naming: (R: report / P: prototype / D: demonstrator)

wk: week number

Q: quarter