1. Goal of the meeting
Make a status of the VALMEM project.

2. Attendees
Emmanuelle Encrenaz  LIP6
Pirouz Bazargan-Sabet  LIP6
Dominique Ledu  LIP6
Laurent Fribourg  LSV
Etienne André  LSV
Remy Chevallier  ST

3. Summary of the meeting

3.1. Prolongation of VALMEM project
The prolongation request of one year has been accepted by the ANR.

3.2. LIP6: Automated translation of VHDL with timings into timed automaton format (HyTech)
A. Bara has been hired for one year on this topic.
The up and down transitions have been modeled. Following to the results found during BlueBerries project we know that this accuracy is mandatory.
A subset of the VHDL language for concurrent and process structures are supported according to the subset generated by the transistor abstraction tool.
3 examples tested:
• Exp1: the HyTech netlist has been generated and executed. However, an optimization of the netlist is mandatory otherwise HyTech is facing model size limitations.
• SPSMALL BlueBerries: the netlist has been generated but HyTech cannot support it
• SPSMALL VALMEM: The netlist has been simplified but HyTech cannot support it

Limitation of the tool:
• Bit: no bit vectors
• Processus structures are limited (but fits to the current requests)
• The model includes 2 delays (rise and fall): it is quite costly but mandatory
• Explosion of the models: cannot be supported by HyTech
  → Use another tools instead of HyTech as UPPAAL or with another tool (IMITATOR2)

Next steps:
Build a traductor for UPPAAL
Test infrastructure for generated files (VHDL + timings…)

3.3. LIP6: Status on Transistor Abstraction
Extraction tool Mygal supports SPSMALL netlist.
The performances are the following:
Spsmall 1 word of 2 bits → 2s
Spsmall 2 word of 2 bits → 5s
Spsmall 3 word of 2 bits → 10s

Improvements of the tool allow 5X improvement of runtime for the SPSMALL of 3 words of 2 bits.

Next step:
Update the timing file: Patricia will manage this point when she will be back of her maternity leave.
Start analysis of SPREG, but the number of bit shall impact the performances
The pattern matching should be mandatory to support the sense-amplifier.

3.4. LSV: Prototype called IMITATOR
A new verification tool integrating the rules plus an optimized formal tool to replace HyTech is under development.

4. Actions
   • Administrative
     o Follow-up the ‘Accord de consortium’ story (All) [asap]
   • Build verification environment for the VHDL translator (LIP6)
   • Start SPREG abstraction (LIP6)
   • Model timings of SPSMALL (LIP6)
   • Improve prototype by replacing Hytech with a new engine (LSV)

5. Next meeting
The next meeting is planned in Crolles in October/November.
### 6. Deliverable overview

<table>
<thead>
<tr>
<th>No.</th>
<th>Title</th>
<th>Deliv.</th>
<th>Resp.</th>
<th>Target</th>
<th>status</th>
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<tbody>
<tr>
<td>D1.1</td>
<td>State of Art in eSRAM conception</td>
<td>R</td>
<td>ST</td>
<td>0→6</td>
<td>Done</td>
</tr>
<tr>
<td>D1.2</td>
<td>Build web site for the project</td>
<td>R</td>
<td>LIP6</td>
<td>0→6</td>
<td>Done</td>
</tr>
</tbody>
</table>
| D1.3 | Description of the conception flow applied on a study                 | R      | ST    | 6→12   | Study 1 done  
Study 2 done  
Study 3 not started  
Run time of conception flow done |
| D2.1 | State of art in memory verification methodologies                      | R      | LIP6  | 0→6    | Done                                        |
| D2.2 | Definition of a new functional and timed model                        | R      | LIP6  | 0→6    | Done                                        |
| D2.3 | Mixing of abstraction methods and temporal characterization           | R      | LIP6  | 6→12   | Done                                        |
| D2.4 | Abstraction tool prototype                                            | P      | LIP6  | 12→24  | ongoing                                    |
| D3.1 | Temporal automaton modeling adapted to memory                         | R      | LSV   | 6→12   | Done                                        |
| D3.2 | Temporal automaton model checking adapted to memory                   | R      | LSV   | 12→18  | Done                                        |
| D3.3 | Verification tool prototype                                           | P      | LSV   | 12→24  | Done                                        |
| D4.1 | Description of the conception flow applied on other studies           | R      | ST    | 12→18  | Not started                                 |
| D4.2 | Experimentation of prototypes on real study                           | R & D  | ST    | 18→36  | Not stated                                  |
| D4.3 | Comparison of results from current verification methods and new methods | R      | ST    | 30→36  | Not started                                 |

The targets are described in months.

Delivery naming: (R: report / P: prototype / D: demonstrator)
wk: week number
Q: quarter