VALMEM meeting (ANR project)

Meeting minutes 12/12/2008

Remy Chevallier 042/63/25 eSRAM team / Crolles1

1.Goal of the meeting

Make a status of the VALMEM project.

2. Attendees

Patricia Renault	LIP6
Emmanuelle Encrenaz	LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

3. Summary of the meeting

3.1.Communication with the ANR: status on 'accord de consortium'

No progress. Need feedback from the lawyer department in ST and CEA. Patent submission seems very complex at legal point of view: Target canceled.

3.2.LIP6: Status on Transistor Abstraction

Support of SPSMALL 3wordsx2bits automatically:

Improvement of color algorithm:

- To resolve the conflict in the memory array, the color algorithm has to go through latch. The latches are now supported. The algorithm used is quite costly (3ⁿ with n is number of Boolean equation).
- Some registers are using latch with internal conflict. These structures are now supported.

One last issue has been faced: in one key part of the design, 2 conflict parts are interconnected. The possible solutions are under study.

At the end of January, the LIP6 will provide the last part of the SPSMALL: read mechanism. LIP6 will provide all the memory for end of March.

3.3.LSV: Prototype called IMITATOR (D3.3)

3.3.1.1.Status

Due to HyTech limitations, the complete SPSMALL cannot be supported. A new strategy is developing by the LSV.

The idea is to provide a set of timing which is providing the right behavior: mainly the timings included in the specification.

The tool is computing the limit of the timing parameters in order to avoid a bad behavior of the design for each internal point.

The first advantage of this strategy is to model just the used part of the design.

However, if another path is providing a good behavior of the design, the tool will remove it. The verification of the write part of the SPSMALL takes 90min.

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Today, this propotype is using HyTech tool. The major part of the time is used by Hytech to build the automaton network. The next step is to replace Hytech by a new dedicated engine which supports dynamic generation of the automaton network.

3.3.1.2.Paper

Paper presented on this prototype: September at Workshop on Reachability Problems

3.4.Review paper for DATE09

Paper has been rejected:

- More experiment result needed
- More formalization for functional abstraction
- Proof of the correctness of the verification algorithm

We planned to submit an updated paper to DATE 2010.

4.Actions

- Administrative
 - o Follow-up the 'Accord de consortium' story (All) [asap]
- Provide delivery D2.4 about the abstraction prototype (LIP6) [wk52]
- Provide read structure of SPSMALL3x2 (LIP6) [wk05]
- Provide abstraction of SPSMALL3x2 (LIP6) [wk09]
- Preliminary analysis of SPREG (LIP6) [March (wk10) → September(wk40)]
 Check the scalability of the abstraction strategy.
 Compare with the tool before the VALMEM project
- Continue the theoretical study of the principles of the verification tool: Study of the termination of the algorithm in the general case: supporting loops in location (LSF) [wk18]
- Improve prototype by replacing Hytech with a new engine (LSF) [wk35]
- → Extra time requested for the project: 6 months Define during the year if a visit at ST is suitable.

5.Next meeting

The next meeting is planned in Crolles in mid-January.



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6.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0>6	Done
D1.2	Build web site for the project	R	LIP6	0 → 6	Done
D1.3	Description of the conception flow	R	ST	6 → 12	Study 1 done
	applied on a study				Study 2 done
					Study 3 not started
					Run time of conception flow
					done
D2.1	State of art in memory verification	R	LIP6	0 → 6	Done
	methodologies				
D2.2	Definition of a new functional and	R	LIP6	0 → 6	Done
	timed model				
D2.3	Mixing of abstraction methods and	R	LIP6	6 → 12	Done
	temporal characterization			_	
D2.4	Abstraction tool prototype	P	LIP6	12 → 24	ongoing
D3.1	Temporal automaton modeling	R	LSV	6 → 12	Done
	adapted to memory				
D3.2	Temporal automaton model checking	R	LSV	12 → 18	Done
	adapted to memory				
D3.3	verification tool prototype	P	LSV	12→24	Done
D4.1	Description of the conception flow	R	$\frac{ST}{T}$	12 > 18	Not started
	applied on other studies				
D4.2	Experimentation of prototypes on	R & D	ST	18 → 36	Not stated
	real study	_	~		
D4.3	Comparison of results from current	R	ST	30→36	Not started
	verification methods and new				
	methods				

The targets are described in months.

Delivery naming: (R: report / P: prototype / D: demonstrator)

wk: week number

Q: quarter