1. Goal of the meeting

The main topics for the meeting are:

- Status on current tasks:
  - T2.4: Abstractor prototype (LIP6)
  - T3.2: Model-checking with optimized timed automaton (LSV)
  - T3.3: Verification prototype (LSV)

- Status on deliverables T0+18:
  - T3.2: Model-checking with optimized timed automaton (LSV)

- Document to provide to the ANR T0+18:
  - Each partner: Provide summary document and the cost of the project for this period

- Prepare meeting with the ANR planned for the 12th September: each partner have to provide 10 slides with his collaboration to the project for the 18 first months of the project

2. Attendees

Patricia Renault  
Emmanuelle Encrenaz  
Pirouz Bazargan-Sabet  
Dominique Ledu  
Laurent Fribourg  
Etienne André  
Remy Chevallier

3. Summary of the meeting

3.1. Communication with the ANR: status on ‘accord de consortium’

No progress. Need a feedback from the lawyer department in ST and CEA

3.2. Status on Deliverables

3.2.1. T2.4: Abstractor prototype (LIP6)

- Pattern matching algorithm has been studied by 2 trainees. Signature and branch algorithms are developed. However, a case is not supported, thus the algorithm must be improved.
- Color algorithm implemented in the abstractor prototype: Abstraction performed in SPSMALL in few seconds (between 6s and 40s depending on net list parsing strategy)
- Next: Try to solve loop conflicts automatically (mainly eSRAM memory points) by a dedicated algorithm
3.2.2. T3.2: Temporal automaton model checking adapted to memory D3.2 (LIP6)

- Spice simulation runs on each gate is included in the abstractor prototype
- However in dedicated cases, few elementary bricks must be plugged together in order to run the timing simulation and provide a consistent model

The transistor abstraction prototype generates the 3 elementary bricks in blue, black and green. The timing analysis of each brick independently does not make sense. The analysis of the complete structure is mandatory.

- Next: build automatically the complex bricks and run the transistor based simulation on them.

3.2.3. T3.3: Verification prototype (LSV)

- The verification prototype generates automatically the timed automaton for VHDL instantiations. The VDHL process is not supported today.
- With this prototype, the ‘trial before study1’ and a part of the study1 have been verified as following:
  - According to the specification behavioral constraints (ie what is a write/read cycle) and timing constraints (cycle time…) are modeled.
  - The verification tool Hytech, generates the next step from a working one, and lists the behaviors which do not follow the behavioral and/or the timing constraints.
  - The behaviors, which are not allowed, induce additional constraints on parameters (setup, hold, cycle time, access time).
  - The additional constraints must be compared to the timings in the specification in order to know if the design performances are improved or not.
- Next: use the prototype on a complete SPSMALL of one word of one bit.

3.3. Prepare review with ANR planned the 11th September in Paris

- First draft for the slides has been presented by LIP6 and ST. A global presentation of 40 minutes is planned for the review.

4. Actions

- Administrative
  - Follow-up the ‘Accord de consortium’ story (All) [asap]
- Provide the summary document (All) [end June]
- Provide the cost document (All) [end June]

- Prototypes development
  - Loop analysis (LIP6) [September 2008]
  - Delay computation (LIP6) [September 2008]
  - Run verification prototype on full SPSMALL with one word of one bit (LSV) [September 2008]
  - Provide deliverable D3.2 (LSV) [September 2008]
  - Support generated process statement in VHDL (LSV) [September 2008]

- Prepare ANR meeting in September
- Provide summary of the work performed (All) [week 27]
- Prepare paper for DATE. First planned provided by email (LSV) [week 24]

5. Next meeting
The next meeting is planned at ST office in Crolles during week 35.

6. Deliverable overview

<table>
<thead>
<tr>
<th>No.</th>
<th>Title</th>
<th>Deliv.</th>
<th>Resp.</th>
<th>Target</th>
<th>status</th>
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<tbody>
<tr>
<td>D1.1</td>
<td>State of Art in eSRAM conception</td>
<td>R</td>
<td>ST</td>
<td>0→6</td>
<td>done</td>
</tr>
<tr>
<td>D1.2</td>
<td>Build web site for the project</td>
<td>R</td>
<td>LIP6</td>
<td>0→6</td>
<td>done</td>
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<tr>
<td>D1.3</td>
<td>Description of the conception flow applied on a study</td>
<td>R</td>
<td>ST</td>
<td>6→12</td>
<td>Study 1 done, Study 2 done, Study 3 not started, Run time of conception flow done</td>
</tr>
<tr>
<td>D2.1</td>
<td>State of art in memory verification methodologies</td>
<td>R</td>
<td>LIP6</td>
<td>0→6</td>
<td>done</td>
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<tr>
<td>D2.2</td>
<td>Definition of a new functional and timed model</td>
<td>R</td>
<td>LIP6</td>
<td>0→6</td>
<td>done</td>
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<tr>
<td>D2.3</td>
<td>Mixing of abstraction methods and temporal characterization</td>
<td>R</td>
<td>LIP6</td>
<td>6→12</td>
<td>done</td>
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<tr>
<td>D2.4</td>
<td>Abstraction tool prototype</td>
<td>P</td>
<td>LIP6</td>
<td>12→24</td>
<td>ongoing</td>
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<tr>
<td>D3.1</td>
<td>Temporal automaton modeling adapted to memory</td>
<td>R</td>
<td>LSV</td>
<td>6→12</td>
<td>done</td>
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<tr>
<td>D3.2</td>
<td>Temporal automaton model checking adapted to memory</td>
<td>R</td>
<td>LSV</td>
<td>12→18</td>
<td>ongoing</td>
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<tr>
<td>D3.3</td>
<td>Verification tool prototype</td>
<td>P</td>
<td>LSV</td>
<td>12→24</td>
<td>ongoing</td>
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<tr>
<td>D4.1</td>
<td>Description of the conception flow applied on other studies</td>
<td>R</td>
<td>ST</td>
<td>12→18</td>
<td>Not started</td>
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<tr>
<td>D4.2</td>
<td>Experimentation of prototypes on real study</td>
<td>R &amp; D</td>
<td>ST</td>
<td>18→36</td>
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<tr>
<td>D4.3</td>
<td>Comparison of results from current verification methods and new methods</td>
<td>R</td>
<td>ST</td>
<td>30→36</td>
<td>Not started</td>
</tr>
</tbody>
</table>

The targets are described in months.
Delivery naming: (R: report / P: prototype / D: demonstrator)
wk: week number
Q: quarter