



Meeting minutes

18/03/2008

1. Goal of the meeting

The main topics for the meeting are:

- Communication with the ANR: status on ‘accord de consortium’
- Deliverable status:
 - D2.4: Abstractor tool prototype (LIP6)
 - D3.2: Temporal automaton model checking adapted to memory (LIP6)
- Planning of next tasks and deliverables

2. Attendees

Patricia Renault	LIP6
Emmanuelle Encrenaz	LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

3. Summary of the meeting

3.1. Communication with the ANR: status on ‘accord de consortium’

The ‘Accord de consortium’ is a document which describes the rules between each partner and the patents.

At ST side, the legal department has taken the ownership of this task. A proposal has been sent to the CEA and is under-study. One open point is still under-discussion on patents.

3.2. Status on Deliverables

3.2.1. Abstraction tool prototype D2.4 (LIP6)

According to the preview meetings, the data structure of the tool has been implemented. The general abstraction mechanism, formal recognition of logic functions without conflict has been implemented.

In order to support logic with conflict, there are 2 solutions:

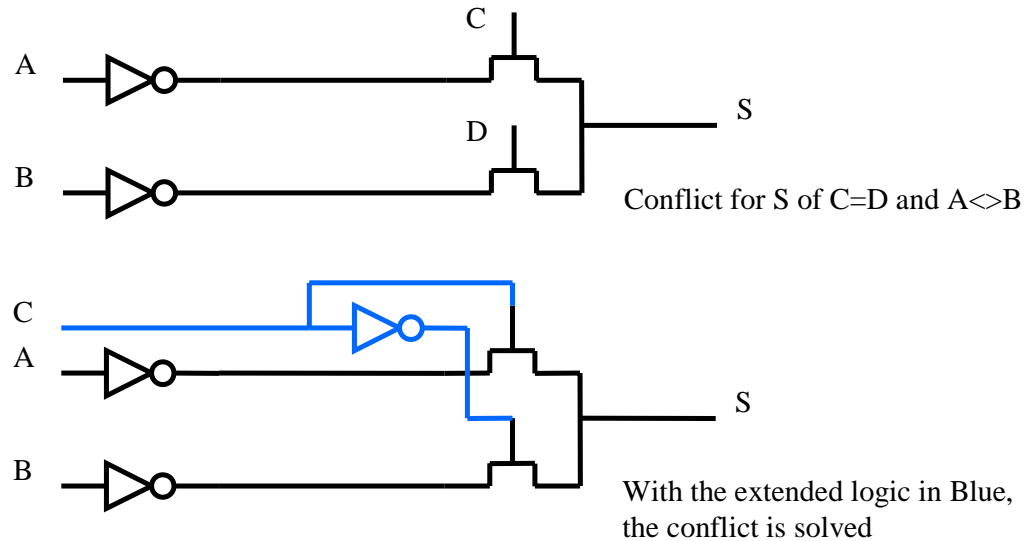
1. Implement pattern-matching algorithm: detect a transistor structure and replace it with a dedicated functionality provided by the designer. This methodology is very efficient, but the functionality is not generated automatically, which could induce errors in the output models



Meeting minutes

18/03/2008

2. Implement 'color' algorithm: In order to solve the conflict gate, the tool has to extend the transistors taken into account in the functionality in order to solve the conflict:



However, this kind of algorithm is very costly and the memory used increase very quickly.

Thus the LIP6 has decided to implement an innovative algorithm. In a first step, the tool parses the netlist from the inputs and defines a new 'color' when a new functional branch arises in the design. When the inputs part of the design under study is reached, the colors collected drives the extend algorithm in order to take into account just the needed transistors.

The planning is the following:

1. Generate the block by abstracted functions and run spice simulations
2. Implement color algorithm
3. An internship is starting on pattern matching implementation

With the color engine, the LIP6 plans that they can handle the SPSMALL testcase automatically by the end of June. The pattern matching algorithm could be useful for the second testcase.

3.2.2.D3.2: Temporal automaton model checking adapted to memory (LIP6)

According to the timed modeling chosen, verifications have been performed on a sub-part of the SPSMALL generated manually by the LIP6.

The automata have been defined as following:

- One VHDL affectation induces one automaton
- 1 clock is used by automaton
- No clock sharing
- Each automaton are deterministic in timings and functionalities

However, in the global model of the eSRAM, if 2 events arise at the same time (critical case of signal races), the 2 cases are checked by the tool.

The design under-study is defined as two latches plugged together.

**Meeting minutes**

18/03/2008

Verification with timings defined as parameters for each gate has been performed. It takes 24 hours. However, if the timings of each gate are modeled as fixed values, the verification is performed in few seconds.

At industrial point of view, we know the delay of each gate. We are looking for optimal values for our timings in the specification.

The LSV is planning an automated modeling of LIP6 output by the end of June.

4.Actions

- Follow-up the 'Accord de consortium' story (All) [asap]
- Develop color algorithm for abstraction (LSV) [June 2008]
- Provide complete abstraction of SPSMALL (LSV) [June 2008]
- Improve verification modeling (LSV) [June 2008]
- Automate verification modeling (LSV) [June 2008]

5.Next meeting

The next meeting is planned at LIP6 office the week 23 or 24 or 25 in 2008.

6.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	done
D1.2	Build web site for the project	R	LIP6	0→6	done
D1.3	Description of the conception flow applied on a study	R	ST	6→12	Study 1 done Study 2 done Study 3 not started Run time of conception flow done
D2.1	State of art in memory verification methodologies	R	LIP6	0→6	done
D2.2	Definition of a new functional and timed model	R	LIP6	0→6	done
D2.3	Mixing of abstraction methods and temporal characterization	R	LIP6	6→12	done
D2.4	Abstraction tool prototype	P	LIP6	12→24	ongoing
D3.1	Temporal automaton modeling adapted to memory	R	LSV	6→12	Slides presented report ongoing
D3.2	Temporal automaton model checking adapted to memory	R	LSV	12→18	ongoing
D3.3	verification tool prototype	P	LSV	12→24	ongoing
D4.1	Description of the conception flow applied on other studies	R	ST	12→18	Not started
D4.2	Experimentation of prototypes on real study	R & D	ST	18→36	Not stated
D4.3	Comparison of results from current verification methods and new methods	R	ST	30→36	Not started

The targets are described in months.

Delivery naming: (R: report / P: prototype / D: demonstrator)

wk: week number

Q: quarter