



**Meeting minutes**

15/10/2007

## 1. Goal of the meeting

The aims of the meeting are to:

- Round table. Welcome to the new comers
- Communication with the ANR
- Status on deliverables
- Next steps
- Next deliverables
- Status of the first study modeling by LIP6

The meeting has been done at ST office in LIP6 office the 12<sup>th</sup> October 2007.

## 2. Attendees

Patricia Renault	LIP6
Emmanuelle Encrenaz	LSV/LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

## 3. Summary of the meeting

### 3.1. Round table

Dominique Ledu Joins the LIP6 as an expert in transistor abstraction and timing analysis at the transistor level.

Etienne André Joins the LSV for a PhD in order to help the modeling and the verification processes with formal automaton.

Welcome to Dominique and André and I wish the best in their new functions.

### 3.2. Communication with the ANR

A new document called 'Etat du consortium' has been received by each partner. This document is dealing with the protection of laboratories' and ST's data and works. Laurent will contact the ANR in order to have more pieces of information on the way to fill this document.

### 3.3. Status on deliverables

According to the last release of the VALMEM ANR project, the deliverable D1.2 is changed to "provide a Web Site of the project" task. The studies are now included inside the deliverable D1.3.

#### 3.3.1. Deliverable D1.3

The study 2 has been presented during this meeting. It deals with a complex high speed eSRAM which is a part of the current commercial ST offer in C65. Thus, for strategic reasons, the slides of this study are confidential. However, for the delivery



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D1.3, a non-confidential description of this eSRAM will be written for the web site of the project.

According to all partners the study2 is much more complex than the study1. The latter must be fully supported automatically before starting the study2.

It might append that the data format provided by the LIP6 must be compacted by an intermediate step in order to help the modeling and verification process performed by the LSV.

### **3.3.2.Deliverable D2.2**

The LIP6 has provided and presented the approach for the functional and temporal modeling.

Formal abstraction method will be used to compute the logic gates. Pattern recognition method will be used to detect analog structure search as sense-amplifiers and latches with conflict search as eSRAM memory point.

The timing model includes all the arcs with the change of the output with only one transition.

In a first step, the timings will be computed by simulations of each sub-block detected by the abstraction process of the eSRAM with the input and output loads.

In order to improve the accuracy, the simulations could be ordered in order to run the simulation of a block when the input slopes are computed from the previous cells.

### **3.4.Next steps**

According to the planning described in the project, a prototype of the abstraction engine with timing characterization is planned for January 2009.

However, the first short term challenge is to define communication format for the design functionalities and timings between LIP6 and LSV. IN order to achieve this, the next step has been decided:

1. Provide a first example with few gates and timings (week46) to start communication loops between the 3 partners in order to define the database format.
2. Provide a part of the study1 at the end of January (week3) in order to check the performances of the LSV engine on a more realistic circuit.

### **3.5.Next deliverables**

- D1.3: Flow description for the study1 with run times for each step. (ST)
- D2.3: Abstraction methodology used with eventually the data structure chosen. (LSV)
- D3.1: Automate format description. (LIP6)

### **3.6.Status of the first study modeling by LIP6**

LIP6 has access to Cadence tool called Opus which is very useful to print the transistor based schematics. Moreover, ST uses this format internally. This is good news for our data exchanges.

A new parser of the spice netlist (with transistors and parasitic) has been developed by the LIP6. Its aim is to read the data before the abstraction step itself.

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**4.Actions**

- Contact ANR in order to have more details about the ‘Etat du consortium’ document (Laurent) [week42]
- Update the document according to Laurent’s feedback (all) [week43]
- Provide short circuits to the LSV in order to start the iteration loop to define a common exchange data format (Patricia, Remy) [week46]
- Provide to the LSV with the new common exchange data format a part of the first study (LIP6) [year 2008 week3]
- D1.3: Flow description for the study1 with run times for each step. (ST) [week50]
- D2.3: Abstraction methodology used (LSV) [week50]
- D3.1: Automate format description. (LIP6) [week50]

**5.Next meeting**

The next meeting is planned at ST office in Crolles the 13<sup>th</sup> December 2007.

**6.Deliverable overview**

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	done
D1.2	Build web site for the project	R	LIP6	0→6	done
D1.3	Description of the conception flow applied on a study	R	ST	6→12	Study 1 done Study 2 done Study 3 not started Run time of conception flow ongoing (wk50)
D2.1	State of art in memory verification methodologies	R	LIP6	0→6	done
D2.2	Definition of a new functional and timed model	R	LIP6	0→6	done
D2.3	Mixing of abstraction methods and temporal characterization	R	LIP6	6→12	ongoing (wk50)
D2.4	Abstraction tool prototype	P	LIP6	12→24	Not started
D3.1	Temporal automaton modeling adapted to memory	R	LSV	6→12	ongoing (wk50)
D3.2	Temporal automaton model checking adapted to memory	R	LSV	12→18	Not started
D3.3	verification tool prototype	P	LSV	12→24	Not started
D4.1	Description of the conception flow applied on other studies	R	ST	12→18	Not started
D4.2	Experimentation of prototypes on real study	R & D	ST	18→36	Not started
D4.3	Comparison of results from current verification methods and new methods	R	ST	30→36	Not started

The targets are described in months.

Delivery naming: (R: report / P: prototype / D: demonstrator)

wk: week number

Q: quarter