Laboratoire
Spécification
Vérification

State of Art in eSRAM design and validation flow

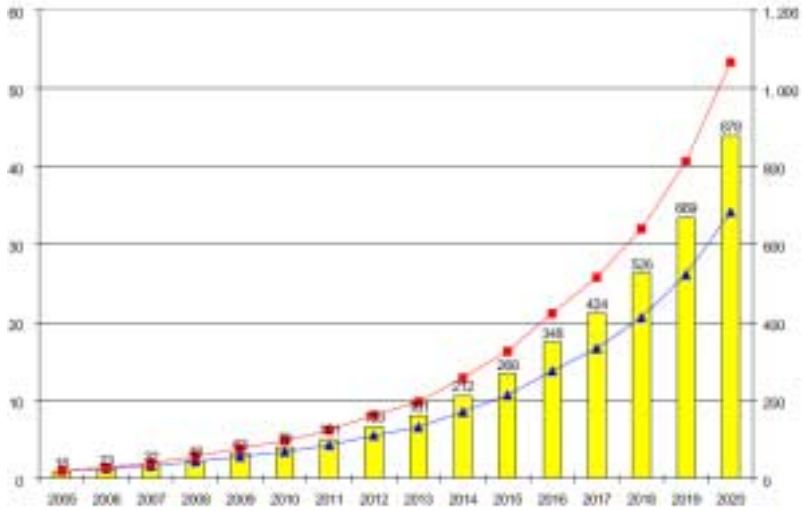
Presentation of D1.1 document

Outline

- Introduction: eSRAM in SoC market
- General overview of the eSRAM design
- Design and verification of transistor based design
  - Design and verification of critical path
  - Design and verification of full cut
- Design and verification of functional view
- Overview of the weaknesses of today flow

Introduction
eSRAM in SoC market

- Number of embedded memory increases with the complexity of the SoC (>400 items).
- Performances and area are key questions for the cost and the performances of the final product.
- Embedded memories are mainly eSRAM



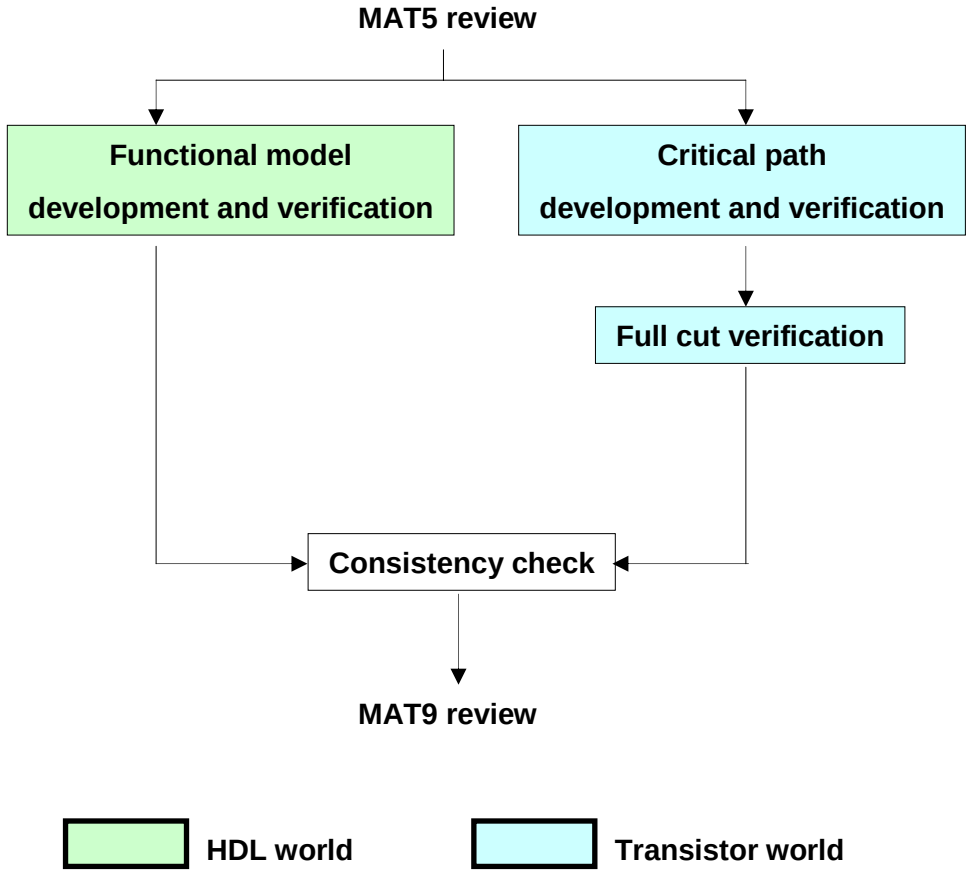
ITRS 2005 System Drivers

General overview of the eSRAM design
Quality items

Quality steps	Description	Development processes to be achieved		
		Specifications	CAD flow	Silicon
MAT5	Memory specification frozen Customers identified	X		
MAT9	Memory compiler ready Basic views built and checked	X	Basic views generated	
MAT10	Additional derived views are generated	X	All views generated	
MAT20	Design successfully checked on silicon	X	All views generated	Functional tests done
MAT30	Design successfully checked on all temperature ranges.	X	All views generated	Reliability test done

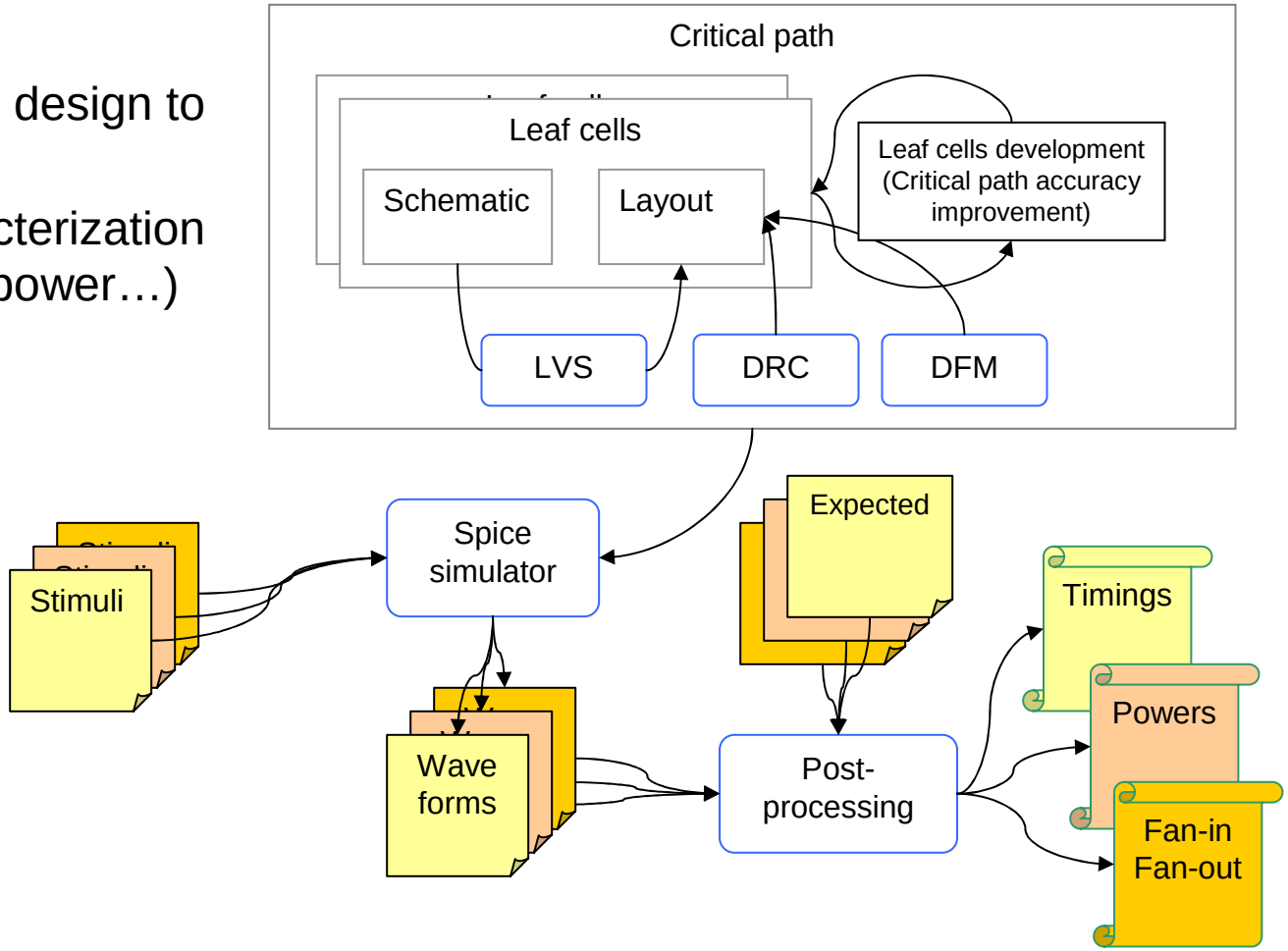
General overview of the eSRAM design
Design flow

- HDL and Transistor worlds are independent: they are compared at the end of the flow
- Transistor based development are spit into 2 steps
  - Tune the model on a simplified eSRAM
  - Compare the results with the real eSRAM



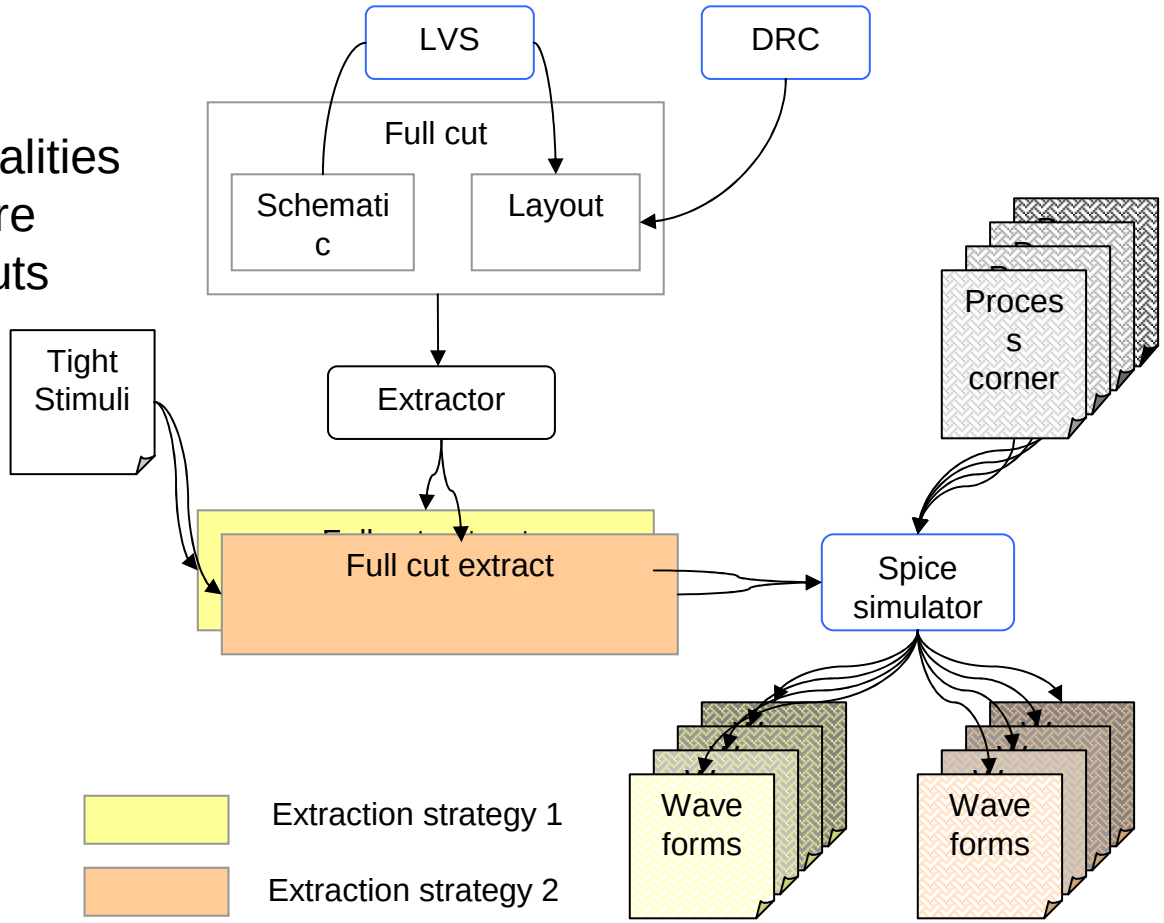
Transistor based design
Design and verification of critical path

- Working on simplified design to win run time
- Perform all the characterization on this design (timing, power…)

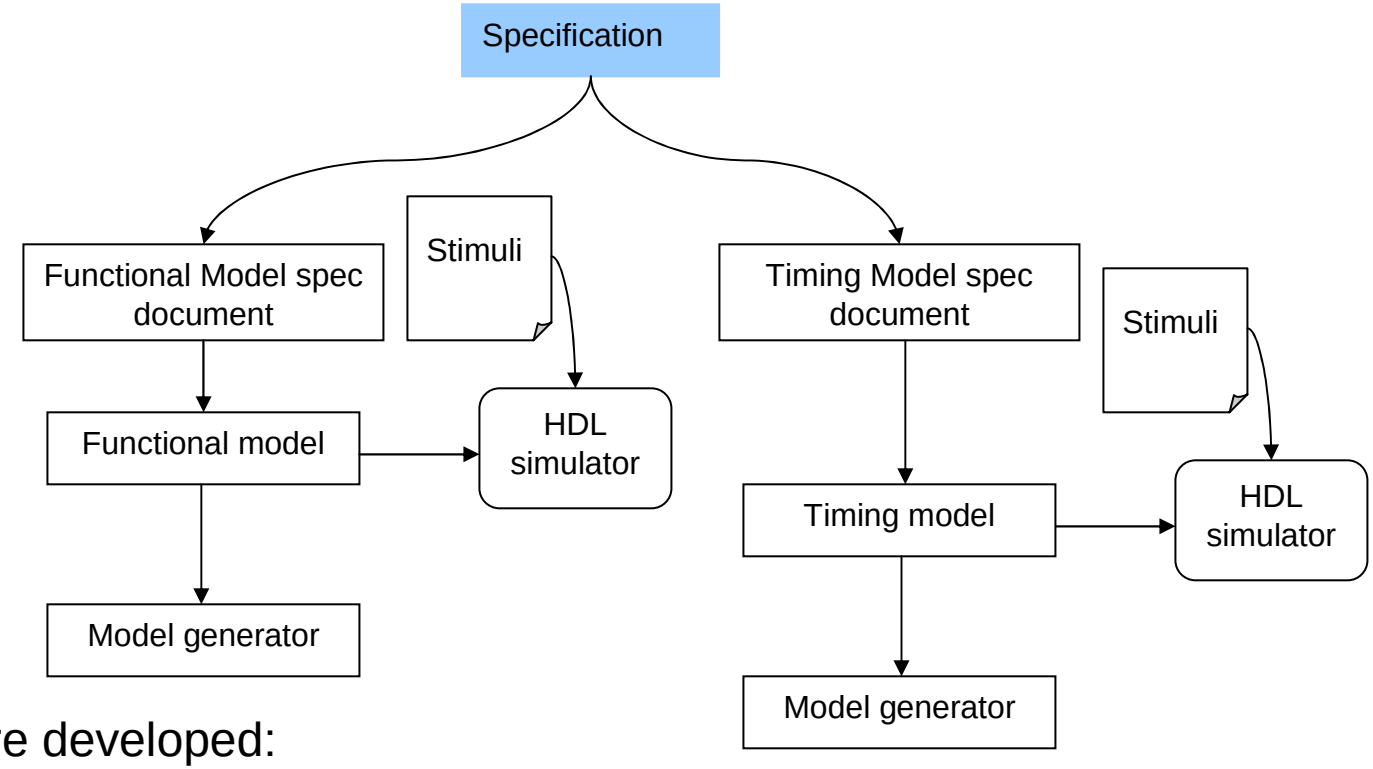


Transistor based design
Design and verification of full cut

Performances and functionalities fund with the critical path are checked in on corner full-cuts



Design and verification of functional view



- Two models are developed:
  - Timed
  - Functional
- Use digital verification strategies

Overview of the weaknesses of today flow (1/2)

Transistor based design flow

- Use only transistor based simulation

  Cannot cover all cases

- Design and vectors are developed by the same people
  - There is no cross-check performed with independent point of view
  - Timings are not optimum
  - All the paths are not checked
  - Debug at silicon must be avoided as soon as possible: very costly, very complex and very long

Overview of the weaknesses of today flow (2/2)

- Need timing study:
  - A kind of static timing analysis
- Need Functional analysis
  - A kind of property checking tool

- Good solution: Check functionalities with timings
  - There is no industrial solutions to check timings and functionalities in one shot